Yield improvement of metal-insulator-metal capacitors in MMIC fabrication process based on AlGaN/GaN HFETs

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Reproducible GaN HFET technology enables the realization of broadband high power amplifiers and highly efficient amplifier concepts such as Class-D, E, F, Doherty, envelope-tracking and other techniques [1]. The fabrication of reliable and low-cost integrated monolithic microwave integrated circuits (MMICs) in general requires high yield of both, transistors and passive elements, i.e. resistors, metal-insulator-metal (MIM) capacitors and inductors. A fabrication of MIM capacitors with high breakdown field strength has been discussed extensively in literature as a stand-alone task or in conjunction with the other technologies, such as GaAs, InP, CMOS [2-4]. In this contribution we will focus on integration of MIM capacitors in the existing AlGaN/GaN HFETs fabrication process flow and discuss technological factors influencing yield and breakdown voltage (V_{br}) of capacitors.

The most commonly used dielectric for fabrication of AlGaN/GaN HFETs is silicon nitride. In FBH standard GaN process flow two layers of SiN_x are applied, namely first for the realization of "embedded" gates and a second for the encapsulation of the gates [5]. The second layer also serves as the dielectric insulator in the MIM capacitors. Both layers are deposited by plasma enhanced chemical vapor deposition at 325 °C, while the exact recipes differ for these layers, mainly due to mechanical stress compensation issue. For wafers used in the experiment targeted thickness of the 2nd SiN_x layer was 200 nm. After in-situ NH_3-plasma pre-treatment the layer has been deposited using SiH_4/NH_3 (2/1) gas mixing rate. The resulting amorphous SiN_x has refractive index in the range 1.86-1.87 as measured by ellipsometry. A typical epitaxial structure GaN:Si/$Al_{0.25}Ga_{0.75}$N/GaN/SiC was used for the fabrication of MMICs with transistors having Ir-based metallization for the gates. On wafer isolation was done by N^+ ion implantation yielding typical isolation resistance of ~ 10^{11} – 10^{12} Ω/□ at 100 V.

As a starting point for optimization we have analyzed MIM capacitor test structures with 160×250 µm^2 top electrode area shown in Fig. 1 and formed between interconnect metallization Ti/Au (20/600 nm) and galvanic Au of 3.5 µm on seeding (base) metal used for the formation of air-bridges. Our MIM breakdown measurements were limited by 200 V and breakdown defined by leakage current limit of 10 µA or damage of the capacitor. The results of measurements on 11 wafers processed in three consecutive runs show the distribution of the mean values in the range from 9 V (σ = 23 V) to 171 V (σ = 16 V) between wafers. In the process of problem identification it was found that the bottom metal roughness is dominant for the observed scattering of V_{br} and reduced yield. Another important weakness is related to the edges of MIM structures. The identified sources of metal roughness are listed below in descending order of importance:

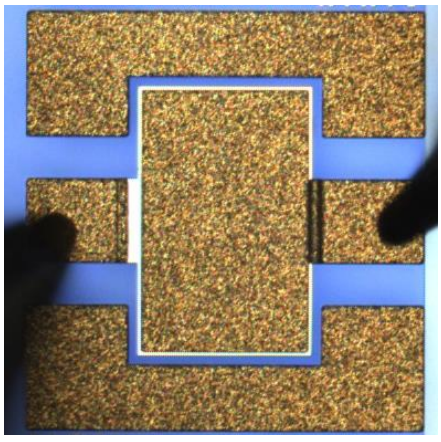

Figure 1. Test MIM capacitor having structure Ti/Au (20/600 nm) - SiN_x (200 nm) -Au (3.5 µm) and 160×250 µm^2 area of the top electrode.

- particles from metal evaporation,
- scratches of metal surface as a result of conventional lift-off procedure,
- semiconductor (GaN in our case) surface defects.

Fig. 2 shows an example of the dark field light microscopy images of the bottom MIM plate after deposition of SiN_x on top of it. The quality of the bottom electrode associated with the metal evaporation procedure has

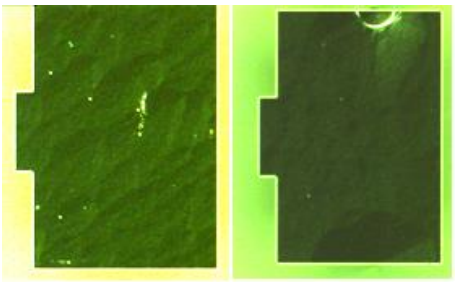

Figure 2. Dark field light microscopy images of the MIM bottom plates showing particles, scratches and epitaxial defects as spots with increased intensity.

been discussed for example by Wang *et al.* [2] where cleaning and pre-melting of a metal source prior each run have been suggested in conjunction with evaporation rate adjustment and post-evaporation treatments. An obvious problem with this approach is the integration of the proposed treatments in the existing process flow and mass-production environment. In addition, in order to increase process stability one should prevent scratches due to lift-off procedure where the thickness of metallization becomes important parameter.

Following the above considerations we have modified the processing sequence of the MIM capacitors by moving the formation of MIM bottom electrodes into a different process step, namely the gate metallization. By doing this we have achieved a few goals simultaneously. First, the total thickness of metallization particularly that of the top Au layer up to ~300 nm has been reduced. This already improves the roughness of the metal surface due to lesser particles. Second, the gentler manual or soak lift-off procedure applied for the gate metallization (and consequently also for the metallization of the bottom capacitor plate) removes numerous scratches from the patterned metal. Third, the top electrode can be formed now by the evaporated 1st interconnect metallization, which was found to be better in terms of edge definition as compared to the 2nd interconnect metal used in previous process. In addition, a soft gate metal annealing at 350 °C after lift-off smoothens the surface of the bottom electrode due to built-in stress reduction by recrystallization.

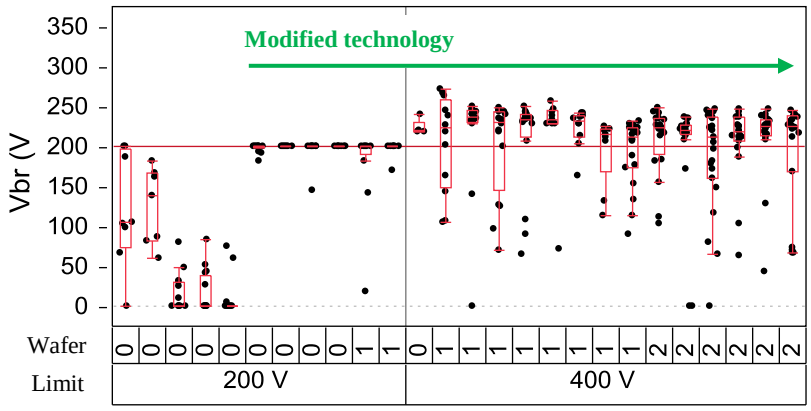

Figure 3. Box-and-whisker plots of MIM capacitor breakdown measurements performed on wafers 01-05 processed before modification and 20 wafers (06-25) processed in 5 consecutive process runs after modification of technology. The measurements were limited by 200 V and 400 V as represented by two groups of plots. The current limit is 10 µA.

Fig. 3 shows the results of our optimization: box-and-whisker plots of the MIM breakdown measurements given for 20 wafers processed in 5 consecutive process runs in comparison to the wafers (wafer 01-05) processed before modification of the technology. A breakdown voltage equal or above 200 V, which indicates breakdown field strength of 1×10^9 V/m, has been measured for 81 % of MIM capacitors. A lowering of the limit for V_{br} to 100 V, which indicates breakdown field strength of 5×10^8 V/m, results in 94 % of MIM capacitors yield. The results of measurements show distribution of the V_{br} mean values and standard deviations in the range from 180 V (σ = 51 V) for wafer 10, where the measurements were limited to 200 V, to 220 V (σ = 56 V) for wafer 16.

In conclusion, we have improved MIM capacitor yield by moving the formation of bottom MIM electrodes into a different process step. This modification does not require additional technological steps being a great advantage of our approach. We achieved yield of 94 % for MIM capacitors with breakdown field strength of 5×10^8 V/m.

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