Diamond-coated High Density Vias for Silicon Substrate-side Thermal Management of GaN HEMTs

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Thermal extraction from III-Nitride power switches would greatly benefit from a high thermal conductivity substrate with a low thermal boundary resistance to the active layer. We have previously reported [1-3] on the electro-thermal benefits of HEMTs capped with nanocrystalline diamond (NCD). However, the thermal path is most critical in the immediate vicinity of the HEMT heat source (drain edge of the gate) which is separated from the diamond cap by the gate contact. In this work, our approach is to bring high thermal conductivity diamond closer to the active gate "from below" by incorporation of a high density of high aspect-ratio diamond-filled through-Si vias (TSV). Figure 1 shows a simulation of a diamond-coated Si via placed directly underneath an AlGaN/GaN HEMT biased at 9 W/mm DC output power, operating at about 15% lower maximum device temperature than a reference HEMT with no diamond.

In three dimensions, a plasma-assisted deposition/etch process can be modeled as a steady-state problem with a deposition/etch rate defined by the precursor diffusion rate in a lithographically-defined geometry. We have applied a multi-step inductively-coupled plasma (ICP) optimization to control TSV shape. TSVs were etched in Si (111) wafers using a SiO_2 mask in a cryogenic ICP dry etch process (-100 °C, 100/5 sccm SF_6/O_2, 1000/9 W ICP/RIE, -56 V DC bias). The etch rate was highly dependent on via diameter (5-230 μm) and exposed Si area (from <5% to >95%), as shown in Fig. 2. However, depth/diameter aspect ratios of up to 18 were routinely obtained with less than 1 hr etch time. Upon seeding with 5-25 nm diameter nanodiamond seed solution, NCD films with 2-3 μm thickness were grown by microwave plasma-enhanced CVD at 750 °C [4]. To improve diamond film uniformity inside high aspect ratio vias, a taper process for the Si sidewall was developed by introducing additional O_2 in the ICP chemistry to increase the sidewall etch rate [5]. A 3° taper angle was experimentally determined to be sufficient for growing diamond on via bottoms at an aspect ratio of up to 9.5, about a factor of 2 improvement over vertical sidewall vias (Fig. 3). This process was implemented on hexagonally-packed circular TSVs helped maximize diamond packing volume and minimize diamond growth time. Figure 4 shows the SEM cross-sections of diamond-coated vias with diameters of 5, 10, and 20 μm, where the additional O_2 in the ICP etch process lead to a wider via opening.

Applied to thermal management of GaN-based transistors, this method has the advantage of providing a substrate-side thermal management solution that avoids critical process steps such as blanket substrate removal. This approach could potentially keep the substrate within bow specifications if diamond is grown selectively inside the vias [8]. Combined with top-side diamond cooling, this process could provide an efficient thermal management solution for power switching GaN devices.

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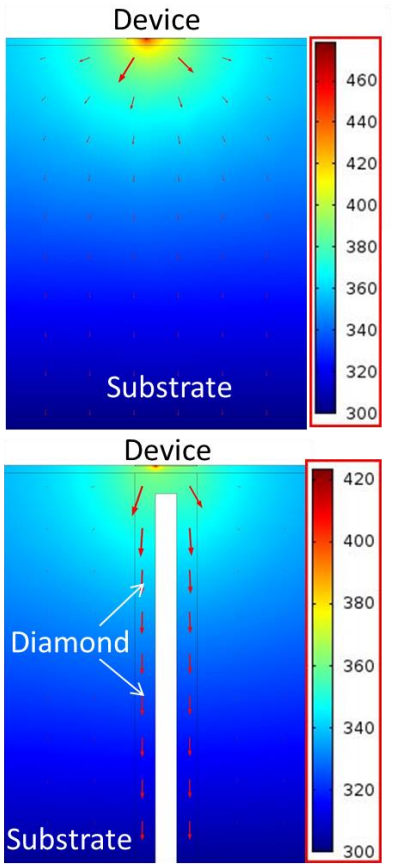

Fig. 1. Heat flow simulation through a Si substrate without (top) and with (bottom) a diamond-coated via placed directly underneath an AlGaN/GaN HEMT biased at 9 W/mm output power.

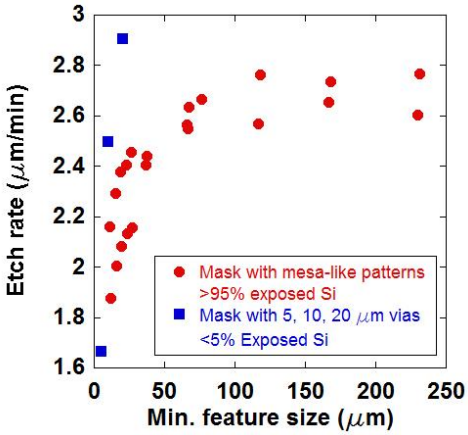

Fig. 2. Si etch rate versus minimum feature size.

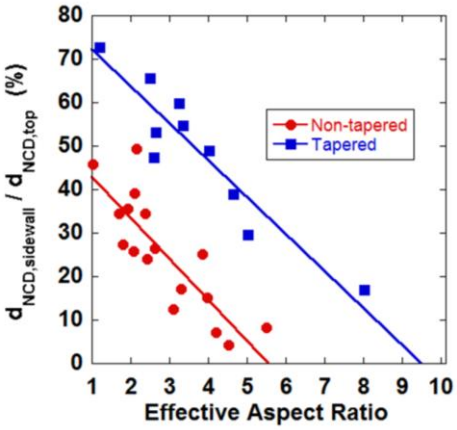

Fig. 3. Aspect ratio improvement by means of via tapering, measured by sidewall diamond thickness as a percentage of top-side diamond thickness at a given diameter and depth (the effective aspect ratio).

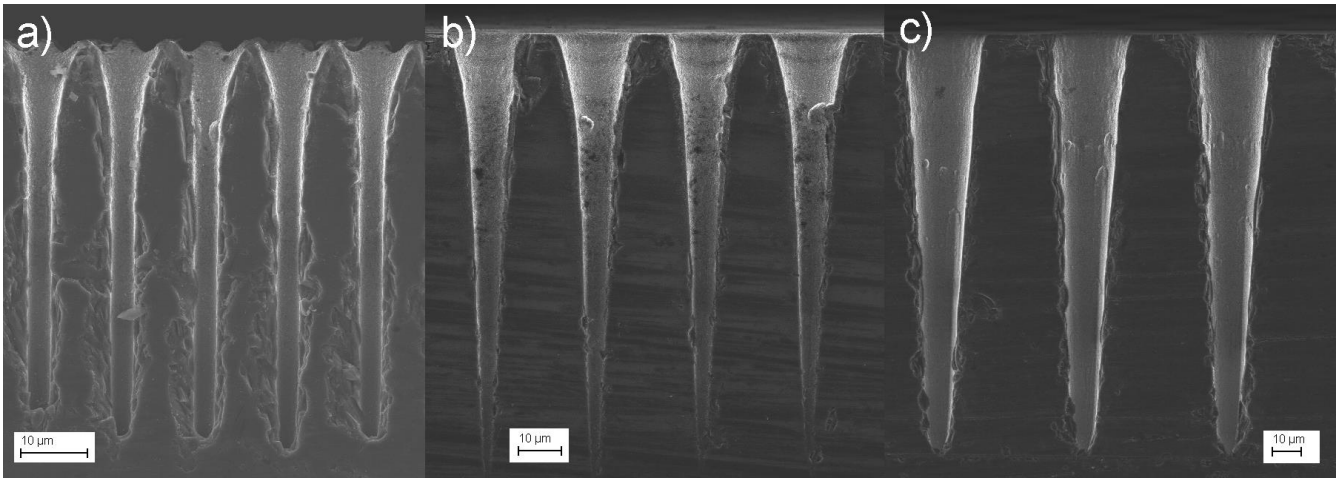

Fig. 4. Cross-sectional profiles NCD-coated vias with a) 5 μm, b) 10 μm, and c) 20 μm nominal top-side diameters. Wider opening diameters were induced by isotropic sidewall etching at a higher O_2 content in the SF_6-based ICP chemistry.