Developing Power Amplifier Module Standards for Reliability Qualification

William J. Roesch
TriQuint Semiconductor, Inc., 2300 N.E. Brookwood Parkway, Hillsboro, Oregon 97124-5300
Phone: (503) 615-9292 FAX: (503) 615-8903 EMAIL: broesch@tqs.com

Background: At JEDEC JC-14.7 meetings over the past twelve years, reliability professionals working with Compound Semiconductors have been discussing an appropriate "JEDEC Standard" for laminate-based Power Amplifier Modules that are currently utilized in cell phones (and any other related volume application for this style of module). In the past, the discussions have compared standard qualification requirements from leading manufacturers and several customers.[1] The requirements are similar from supplier-to-supplier and from customer-to-customer. In the past five years, a Task Group within the Committee for Compound Semiconductor Reliability and Quality (JC-14.7) has been addressing various questions about developing standards, and this work is intended to document the progress and publicize the developments.

1.0 INTRODUCTION

Laminate-based Power Amplifier Modules (PAMs) are a unique application of Compound Semiconductors. PAMs are an enabling component of cell phones that transmit signals with high efficiency, linearity, and reliability that is yet unmatched by other technologies. A typical PAM consists of a substrate, which may be a leadframe, but is usually a laminated multi-layer base. Upon the base, one or more compound semiconductor die are attached. Some PAMs also include silicon die. Additionally, passive components, usually acoustic filters, ceramic capacitors, inductors, and/or couplers are either built-in to the substrate or added as Surface Mount Devices. Finally, the substrate and components are encapsulated using a transfer molding process. Even though these types of modules have been utilized for semiconductors in the past, the use of Compound Semiconductors, with acoustic filters, and a multi-layer laminated substrate, for a relatively high power dissipation application, is clearly unique.

1.1 TIMELINE

2001: JESD26 rescinded.

2002: Standard test battery for PAMs originally suggested
- Ann Fletcher, RFMD, volunteered to lead.

2004: Comparison Matrix, Suppliers & Customer Methods

2005: RFMD Presentation: ***An Overview of Reliability Testing Challenges in Integrated Power Amplifier Modules for Wireless Applications.***
- Lance Rushing, Skyworks, volunteered to lead

2006: Participants volunteered to help: RFMD, Skyworks, Anadigics, Philips, Freescale, M/A Com
- Mike Ferrara, RFMD, volunteered to lead.

2008: Started Current PAM Task Group (IRPS Meeting)
- Bill Roesch, TriQuint, volunteered to assemble topics
- Similar JEDEC documents reviewed.
- List of concerns circulated & ranked (ROCS Meeting)

2009: Top Concerns Discussed (selected three topics)
- Publicity in April/May Compound Semiconductor Magazine

2010: Draft Documents Assembled
- ManTech Panel to discuss standards, Portland, May 18

2011: Document recommendations and changes
- Four revisions and changes
- Final revisions approved at ISTFA Meeting (March)

2012: Qual. Document and RFBL Method balloted
- JEDEC Balloting: February… both passed.
- Developed line-by-line comparisons to JESD47
- Meeting with JC-14.3 to resolve concerns (Sept.2012)

2013: RFBL Method Published as JESD226

2.0 WHY NEW COMPOUND SEMICONDUCTOR STANDARDS?

Following are a few of the reasons for new PAM standards that have been discussed by the Task Group… [2]

A. Consolidate "standard" overall qualification tests, so that all the suppliers and customers can combine efforts and reduce the number of "special" requirements and variants requested by each company. These new requirements would be differentiated from existing documents because of significant differences in 1) incorporated CS technologies, 2) materials, 3) packaging, 4) mechanisms, and 5) the PAM application.

   Originally, PAMs had a natural fit with many aspects of JESD26 (General Specification for Plastic Encapsulated Microcircuits for Use in Rugged Applications). But when JESD26 was rescinded in 2001, the only alternative was the more generic JESD47. Basically, a new set of PAM-oriented qualification tests could be accomplished as…

   i. a whole new JESD47-type document specifically for PAMs (COMMITTEE LETTER BALLOT JC-14.7-12-094). This can be thought of as a replacement of the package-specific qualification of JESD26 with special consideration of the "Telecom Hand Held" application-specific considerations that are modeled in JESD94, or

   ii. a special set of tables for PAMs that blends unique aspects of Table 1a (nonvolatile memory devices) and Table 2 (Qualification tests for components in nonhermetic packages) as in JESD47.

B. Specific methodology specification(s) to define special test method(s) applicable to PAMs? (Similar to any part of JESD22)

   i. For example, an RF biased lifetest document to describe the necessary requirements of applying RF and temperature acceleration. (JESD226)

   ii. For example, an **unbiased** humidity test at conditions such as 85/85 . . .
      a) As an alternative to the humidity saturation and pressure experienced in Autoclave.
      b) As an alternative to the higher temperatures and pressures of Unbiased HAST.

   iii. For example, a special "slow" or "gentle" thermal cycling test to alleviate the pyroelectric failure mechanism generated by fast excursions on SAW components. (JESD22-A104)

   iv. For example, a special "position paper" or "white paper" such as JEP155 to describe ultra ESD sensitivity of PAMs.

   v. For example, a new HALT-type combination test involving vibration and thermal stress using continuous monitoring during aging.

C. A document (Similar to an addition to JEP122 and JESD94) to specifically address different failure mechanisms of PAMs such as:

   i. Unique failure mechanisms for compound semiconductors:
      1) HBT Recombination Enhanced Defect Reaction (REDR)
      2) HBT Kirk effect Induced Breakdown (KIB)
      3) HBT Safe Operating Area (SOA) emit.-collector degradation
      4) HBT Gradual β drift
      5) pHEMT Sinking Gate
      6) GaN Reverse Piezoelectric Effect (RPE)

ii. PAM differences in common failure mechanisms, such as unique N and Ea factors (used in JEP122 and JESD94) for CS components in PAMs. e.g. the "Peck power law model" used for corrosion uses –N as an exponent of Relative Humidity and Ea is the activation energy of the Arrhenius expression such that all acceleration in humidity is based upon N=2.66 and Ea=0.79eV for Aluminum Corrosion per silicon history.

iii. Sub-component failure mechanisms unique to PAMs, such as These for SAW and BAW devices:
1) Pyroelectric Damage (lithium niobate and lithium tantalate)
2) Acoustomigration on resonators and reflectors
3) Mass Loading due to moisture or surface contamination

3.0 RANKING THE ISSUES

Based upon inputs from participating companies, the top areas the JC-14.7 (Compound Semiconductor) Task Group selected were:

FIRST = RF biased lifetest document to describe the necessary requirements of applying RF and temperature acceleration. (Committee Letter ballot JC-14.7-12-093) Published in 2013 as JESD229.

SECOND = A special standard similar to JESD26 and JESD47 with focus on PAMs and unique differences and special requirements with special consideration of Compound Semiconductors. (Committee Letter Ballot JC-14.7-12-094). Approved for re-ballot by JC-14.3 on September 26, 2013. Re-ballot authorized by JC-14.7 on October 14, 2013.

THIRD = Quantifying PAM differences in failure mechanisms and acceleration factors, (similar to JEP122) for both common mechanisms and unique Compound Semiconductor mechanisms. This will require basic science work and publication of results. This area was tabled by the task group until the first two aspects above are established and the research can be completed and published to maintain a synergy of applicability between the three document types.

4.0 PRELIMINARY DISCUSSIONS AND PROGRESS

4.1 RF Biased Lifetest . No one argued that DC bias and RF bias are different in many respects. Specific comparisons between DC bias and RF bias are summarized by a publication.[6] JESD226 has now been published, but temperature is not the only consequence of applying RF bias. The task group anticipates more RF considerations. The peak voltages and currents are likely to have particular accelerating effects that are different than constant DC bias. Many Power Amplifier Modules (PAMs) employ circuitry for different bands and for different power levels – how should each be exercised in an RF biased lifetest? Additionally, the interactions of temperature, voltage, and current have many permutations to be considered. There is a lot of operational space between applying a sine wave on one input and operating a device "*like it runs in a phone*." Various questions need to be settled to help define the subsequent methodology and operational details. (RFBL = RF Biased Life). Following are some of the open questions . . .

A. Does RFBL replace HTOL, or is RFBL an additional test to HTOL?
B. Is RFBL intended to stress thermal and electrical mechanisms as well as all the interactions between temperature and RF bias?
C. Will RF power or temperature be maximized? (which has priority?)
D. Will coverage of nodes operated or the similarity to operating bias be maximized?
E. Is RFBL expected to be monitored during testing, or is it allowed to measure performance during intervals where RF bias is removed?
F. Is preconditioning required?
G. Is burn-in or pre-selection of samples allowed?
H. How is power control to be evaluated? For example, what features of the application need to be considered besides frequency and power level?
I. Should the operational conditions be evaluated to determine the conditions of maximum power dissipation within the PA or maximum peak temperature?
J. Is there an applicable RF bias test that is applicable to individual components utilized within the module, or is RF bias only applicable to the fully assembled module?
K. How should mismatch (SWR) loading aspects be considered and overlayed in addition to RF input parameters?

The task group elected to start with a basic stress method document to introduce RF stress and refine the methodology based upon findings regarding the above questions. This basic outline document was published as JESD226 in February 2013.

4.2 Special Qualification Requirements for PAMs. This is the original Module topic professionals began discussing in the JEDEC committee almost 12 years ago. Every manufacturer seems to have a unique set of tests that are "necessary" for qualification. However, most customers also have a unique set of qualification requirements as well. In order to conduct business with multiple customers, the list of qualification tests quickly expands to a superset of methods, durations, conditions, and sample sizes that becomes prohibitive to complete in terms of time and cost.

The initial strategy for qualification was to define a fundamental set of qualification requirements and then personalize the requirements to the unique aspects of PAMs. The aspects include 1) application specific modeling per JESD94, 2) compound semiconductor and filter technologies, 3) materials, 4) mechanisms, and 5) packaging differences as determined in part 4.3.

4.3 Power Amplifier Failure Mechanisms. The task group recommended starting with humidity induced failure mechanisms involving corrosion shorts and opens. One difference between Compound Semiconductors and silicon devices seems to be in moist environments. There are certainly special challenges for laminate-based modules in traditional humidity testing. JEDEC has recently introduced unbiased versions of HAST methods and labeled Autoclave as "not recommended" for silicon technology. These differences beg the question of an appropriate accelerated test for **modules that incorporate compound semiconductors and acoustic filters in humid environments**. There have been several compound semiconductor publications which have investigated thermal and humidity acceleration – and those publications suggest some significant differences from silicon, particularly for mechanisms on compound semiconductor and acoustic fileter technologies. [3,4,5] The detailed mechanisms have not been explained in these references, so the published science is somewhat lacking here. It has been proposed to utilize JEP122 as a template to identify and expound on the differences. So far, there is not an industry consensus on the "proper" activation energy for compound semiconductors in humidity. Perhaps there are more failure mechanisms at work than the two generalized in the description above (opens and shorts). So far, there is better agreement on the "Peck RH exponent," albeit much higher than reported for silicon devices. The following table compares these two acceleration factors as defined in JESD94 and recent publications on GaAs technologies used in Power Amplifier Modules...

Table 1. Comparison of Humidity Acceleration Factors

	Silicon Lo	Silicon Hi	CS Ref [3]	CS Ref [4]	CS Ref [5]
Activation Energy	0.79eV	0.9eV	1.7eV	2.08eV	0.28eV
Peck RH Exponent	-2.66	-3.0	-10.7	unknown	-11.4

The committee has worked to develop a "matrix" to compare all participating supplier's standards to participating customer's requirements, but so far, this has not resulted in consolidation.[1] It's unclear what method is appropriate to derive the "best" list of qualification tests? In the beginning, suppliers requested a "standard" to reduce the proliferation of tests and conditions, so as to streamline qualifications in both time and cost. [6] However, customers have a different idea of standardization, such as a suite of tests to minimize reliability risk, maverick excursions, and early failure mechanisms – particularly for laminate-based modules.

5.0 Remaining Work.

The Task Group is continuing to investigate findings, models, and issues to address the concerns selected in Section 3. Design of specific test structures and validation from independent laboratories have also been suggested for further investigation. [7]

New precedents in cooperation have just been established between Silicon-based and Compound Semiconductor-based committees within the JEDEC organization which resulted in agreement on balloting a PAM Reliability Qualification Standard. With the completion of a PAM Reliability Qualification Standard imminent, work can now begin to identify and characterize specific failure mechanisms and to refine a set of requirements that are tuned specifically to the unique aspects and applications of Power Amplifier Modules as described in Section 4. The culmination of this development will be a streamlined qualification that addresses specific traits (described in Section 2) of PAMs and the Compound Semiconductors that are typically enabling the performance consumers have grown to expect in their smart phones and wireless devices.

If selected for publication and presentation at the CS MANTECH conference, the history as described in this abstract will be provided and the arguments and data used to establish the new precedents will be showcased.

6.0 REFERENCED JEDEC DOCUMENTS:

These are available from the JEDEC website . . .

JESD47 STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS

JESD22-A101 STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST:

JESD22-A102 ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE:

JESD22-A104 TEMPERATURE CYCLING

JESD22-A110 HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)

JEP155 RECOMMENDED ESD TARGET LEVELS FOR HBM/MM QUALIFICATION

JEP122 FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES

JESD94 APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY

JESD226 RF BIASED LIFE (RFBL) TEST METHOD

7.0 REFFERENCES

[1] William Roesch and Dee Byrd, "Benchmarking Reliability Tests for Plastic Laminate Modules," pp 69-77, 2002 GaAs REL Workshop, Monterey, CA., October 20, 2002. (TriQuint, RFMD, Alpha, Conexant, M/A Com)

[2] Discussion at JEDEC 14.7 Meeting, October 12, 2008, at ROCS Workshop/CSICs Conference, Monterey California.

[3] Peter Ersland, Hei-Ruey Jen, and Xinxing Yang, "Lifetime Acceleration Model for HAST Tests of a pHEMT Process," pp 3-6, 2003 GaAs Reliability Workshop – called the ROCS Workshop after 2003. San Diego, CA. November 9, 2003 (M/A Com)

[4] William Roesch, "Thermal Acceleration of Compound Semiconductors in Humidity," pp 111-122, 2005 ROCS Workshop, Palm Springs, CA., October 30, 2005. (TriQuint)

[5] Leslie Marchut, "Acceleration Factors for THB Induced Degradation of AlGaAs/InGaAs pHEMT Devices," pp 31-40, 2007 ROCS Workshop, Portland, OR, October 14, 2007. (RFMD)

[6] Y. Qu, P. Scott, L. Marchut, & M. Ferrara, "An Overview of Reliability Testing Challenges in Integrated Power Amplifier Modules for Wireless Applications," pp 95-109, 2005 ROCS Workshop, Palm Springs, CA., October 30, 2005. (RFMD)

[7] Discussion at JEDEC 14.7 Meeting, May 20th, 2008, at MANTECH Conference, Tampa Florida.