Homogeneity control of powerelectronic device structures by advanced in-situ metrology

Oliver Schulz[1], Armin Dadgar[2], Jonas Hennig[2], Oliver Krumm[2], Stephanie Fritze[1,2], Jürgen Bläsing[1], Hartmut Witte[2], Annette Diez[2], Alois Krost[2]

[1]LayTec AG, Seesener Strasse 10-13 10709 Berlin, Germany
[2]Institut für Experimentelle Physik, Otto-von Guericke-Universität Magdeburg, Universitätsplatz 2, 39106 Magdeburg, Germany

Semiconductor manufacturers seek for perfection, and that includes trying to produce in-spec devices all across the wafer on every wafer. This equals a 100% yield target across all wafers in all runs, regardless of the material backbone of the devices. To succeed, all device layers need to have a maximum degree of homogeneity in terms of layer thickness, doping, interfaces and surface morphology, and specifically for compound semiconductors devices the ternary and quaternary composition. Variations in these parameters are usually detected subsequently (*ex-situ*) to the deposition process by different and often sophisticated measurement techniques (e.g. XRD, Hall measurements, and many other). This generates a significant part of the production cost due to equipment cost and even more due to the time consumption by these quality control techniques.

In this work, we will show for powerelectronic device structures with focus on the III-N material system that the homogeneity of the most important device parameters can be controlled by advanced *in-situ* monitoring of the main growth parameters during the deposition process, in particular the wafer surface temperature, curvature, and growth rate.

High electron mobility transistors (HEMTs) based on AlGaN/GaN or InAlN/GaN device structures are excellent approaches for the next generation of power electronics, due to their combination of high electron mobility and high critical electric field strength. Their nearly three orders of magnitude lower specific on-resistance (theoretical value) compared to silicon based devices could enable an at least 10-fold reduction of power losses, device size and cost. Especially the use of large diameter silicon substrates opens an additional way for further cost reduction in the production process. Although the growth of high quality GaN layers on Si has been demonstrated in recent years, silicon substrates have one big disadvantage due to the low energy barrier for slip plane generation. For the growth of GaN on silicon compressive stress has to be applied during growth to compensate for tensile thermal stress upon cooling and to avoid cracking of the nitride layer. At GaN growth temperature, however, the compressive stress is increasing with increasing layer thickness and dislocation glide is often observed for thicker layers (Fig. 1). With such plastic deformation of the substrate large ex-situ bow and anisotropy in curvature is observed (Fig. 2). Typically the wafer exhibits a saddle like shape although the measured bow value as defined by SEMI standard remains low.

In this work, we present first results of the correlation between in-situ growth data (curvature and wafer surface temperature), wafer-level data (e.g. XRD, Hall) and the final device performance. It will be shown, that advanced in-situ growth metrology is the key to control the device yield. Several methods to avoid plastic deformations and a large wafer curvature are demonstrated and discussed. Furthermore, composition and doping fluctuations of device layers can be detected already during the growth process. In addition to the results of the process optimization work, we will present in-situ based process control untilizing the latest version of the EpiNet 2 software package. Examples will be given on user-friendly “traffic-light” GUI for operator level and drill-down access for the engineer level for root-cause analysis of variations of the production process.

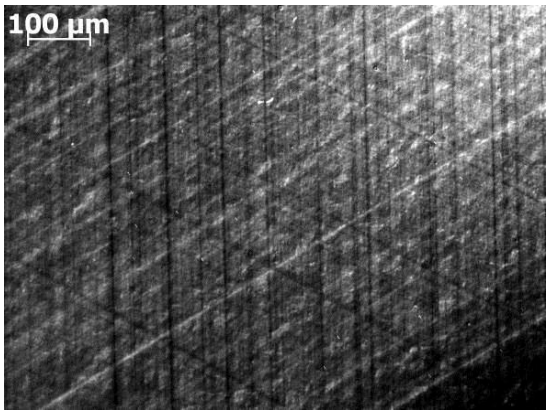

Figure 1: Nomarski microscope image of plastically deformed GaN on Silicon.

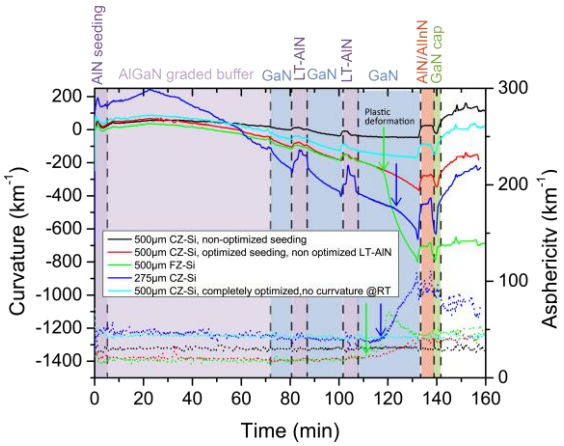

Figure 2: Curvature measurements of an AlInN/GaN HEMT structure grown on Si(111) substrates. The parameter variation (type of substrate, seeding, LT-AlN) is given in the insert (solid). In addition, the asphericity of the wafer is measured simultaneously (dotted).