Implementation of slanted sidewall gates technology in the fabrication of S-, X-, and Ka-band AlGaN/GaN HEMTs.

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Keywords: Ka-band, GaN HEMT, embedded gate technology, ZEP 520A

This work presents the results of slanted sidewall embedded gate technology implementation in a process flow towards S-band discrete devices and X- and Ka-band GaN HEMT MMICs. Transistors with gate lengths of 500 nm and 250 nm were fabricated using both, vertical and slanted sidewall gate technologies. Electrical performance and yield of transistors fabricated on 4 inch 4H-SiC wafers were the same for both technologies. Short-channel effect free Ka-band transistors with a gate length of 100 nm were fabricated using a specially adopted epitaxial structure. The AlGaN barrier layer was thinned down to 12 nm and an additional back barrier layer was added under the GaN channel in order to provide a better current confinement to the 2DEG region.

Table 1 – Epi and process details for different kinds of transistors

Band	Epi details				Process details		
	Cap	Barrier	Channel	Buffer	L_g (nm)	Gate profile	d_{SiNx} (nm)
S	5 nm GaN	25 nm $Al_{0.18}GaN$	850 nm GaN	~1000 nm GaN:Fe	500	Slant/ Vertical	150
X	5 nm GaN	18 nm $Al_{0.25}GaN$	850 nm GaN	~1200 nm GaN:Fe	250	Slant/ Vertical	100
Ka	2 nm GaN	12 nm $Al_{0.32}GaN$	50 nm GaN	~2200 nm $Al_{0.04}GaN$	100	Slant	100

Device heterostructures were grown by low-pressure MOVPE both on n-type and semi-insulating 4H-SiC substrates. Both, inhouse epi wafers and commercially available external wafers were processed together to distinguish between epilayer and process related effects. Table 1 lists the details of the epitaxial layers and basic technological features for devices optimized for the different frequency bands. As the targeted frequency increases the gate length decreases from 500 nm for S-band devices to 250 nm for X-band devices and consequently to 100 nm for Ka-band MMICs. Accordingly, in order to avoid short channel effects the gate length to gate-to-channel distance ratio needs to be maximized. As short gate-to-channel distances are compromising 2DEG electron density the Al concentration in the AlGaN barrier is systematically increased to compensate this effect. All wafers were passivated with SiNx deposited at 325 °C using a Sentech SI500D PECVD tool. For slanted gate fabrication 50% diluted ZEP 520A resist was spun at 2000 rpm and subsequently baked for 3 min at 115 °C, resulting in a final thickness of ~210 nm. After development, resist reflow process was performed at 155 °C during 20 min followed by etching in CHF_3/SF_6 gas mixture. For vertical gate trench technology the etch mask consists of two layers of 300 nm thick ARP 639.10 resist subsequently spun at 5000 rpm towards a final thickness of 600 nm. After development, etching was performed in SF_6/He gas mixture using a Sentech SI500 ICP tool. Size and profile of trench openings in SiN_x were analyzed using scanning electron microscopy (SEM). After wafer processing DC, S-parameter and load-pull measurements were performed in order to obtain electrical properties and estimate the yield of transistors.

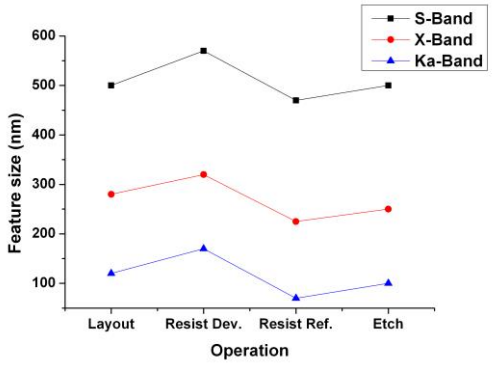

Figure 1 – Actual trench size after different process steps

As it has been shown before [1], the newly developed technology of GaN HEMT gates fabrication using ICP etching with thermally reflowed ZEP 520A as etch resist mask, allows fabrication of gates with dimensions down to 50 nm and sloped sidewall profile. This technology has several advantages compared to the vertical sidewall gate approach: first of all it has a very good flexibility that allows for the fabrication of gates with lengths ranging from 500 nm down to 50 nm using the same resist technology, the second advantage is better trench sidewall coverage with gate metal, which is considered as one of the prerequisites for highly reliable devices [2]. In order to prove reliability and repeatability of slanted gate technology, 7 wafers were processed using vertical and slanted

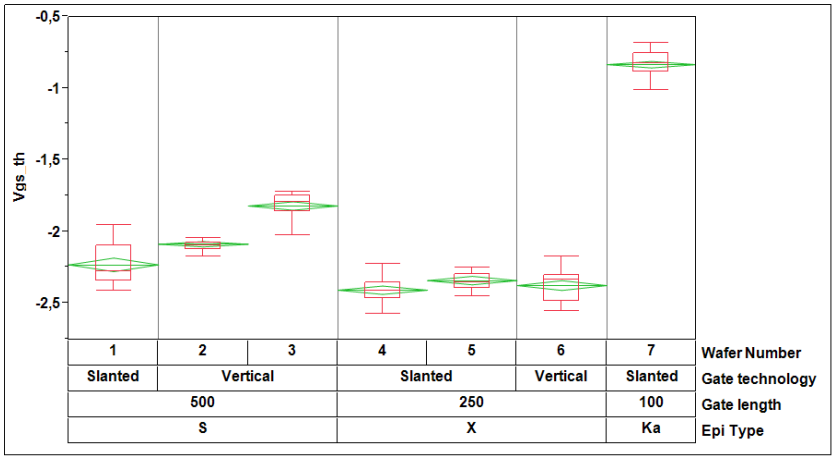

Figure 2. Pinch-off voltage distribution for S-,X- and Ka-band transistors fabricated using different technologies.

gate approaches. Figure 1 shows the gate trench dimensions measured after different process steps. As can be seen, all transistors have the same change in trench dimensions according to the technological operations. This means that the process is practically free of sizing phenomena. After trench fabrication SEM measurements have shown that slanted gate technology provides a good accuracy in terms of trench size (± 10% of nominal gate length), together with trench sidewall slopes in the range of 72 ± 2 deg. First comparison of electrical characteristics was performed immediately after gate fabrication. Figure 2 compares the pinch-off properties of devices fabricated using different gate technologies. All transistors show very similar results on wafers with the same epi design, which means that both gate technologies are comparable in terms of DC-performance of the resulting devices. DC measurements of Ka-band transistors showed V_{th}=-0.8V, I_{DS_max}=0.8 A/mm and g_m=380 mS/mm, which is comparable with state-of-the-art results for AlGaN/GaN transistors with 100 nm gate length [3]. Figure 3 shows the results of load-pull measurements taken from S- and X-band transistors. As can be seen, transistors with slanted gates demonstrate the same behavior as reference transistors at both tested frequencies.

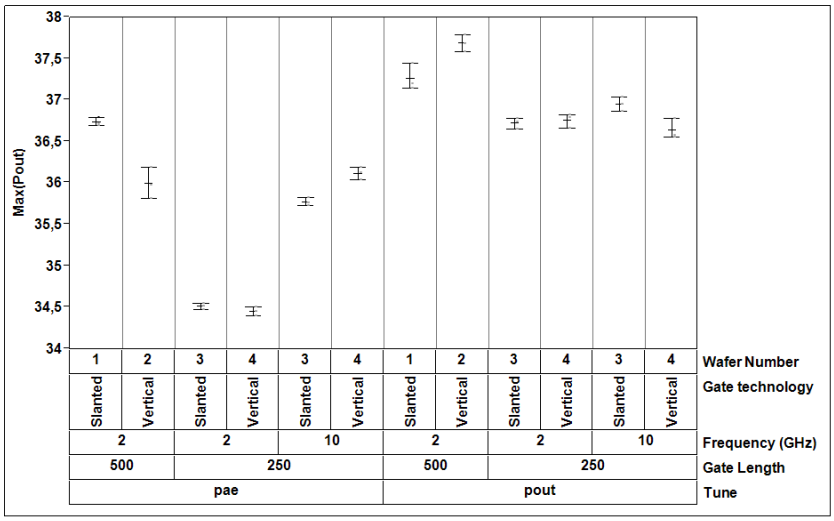

Figure 3. Maximum output power comparison for S- and X-band transistors fabricated using different technologies. S-band devices have been measured at 2 GHz, X-band devices at 2 GHz and 10 GHz frequencies. The abbreviation "tune" refers to the impedance matching during load pull measurements.

The newly developed technology of embedded GaN HEMT gates has recently been implemented in the process flow of S-, X- and Ka-band transistors fabrication. First electrical measurements of DC and large-signal characteristics of S- and X-band transistors showed similar performance for both vertical and slanted sidewall gates. 100 nm gate transistors were fabricated using the newly developed epi design intended for short-channel effect elimination. Preliminary results of DC measurements showed good pinch-off at V_g = -0.8V together with g_m=380 mS/mm and I_{DS_max} = 0.8 A/mm. In conclusion, a robust gate technology module based on ZEP 520A resist technology has been successfully implemented in existing S-, X- and Ka-band GaN processes. Furthermore the epitaxial layer sequence has been adjusted to the specific gate dimensions of transistors optimized for the respective frequency bands.

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