Improvement of Transconductance Flatness of GaAs MESFETs

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The fabrication of amplifiers with good linearity requires a clear understanding of the process. The linearity primarily depends on the flatness of the transconductance curve (Gm versus gate voltage). The surface states between GaAs and the nitride passivation layer [1] as well as the material etching in the ungated area reduce the flatness of the transconductance curve. High gate leakage current of the devices can also degrade the transconductance [2]. However, Gm needs to remain constant in the operating range of the gate bias to achieve low third order intermodulation distortion (IM3) and high third order intercept point (IP3) [3]. In this investigation we optimized the process to obtain flat Gm curves and manufactured amplifiers with high linearity.

GaAs high (+) low (-) high (+) epitaxial structure with InGaP etch stop layer was used for the fabrication of MESFETs. Half micron T shaped gate was formed after standard gate metal deposition and lift-off process.

There are three groups of wafers were used to study the effect of ungated channel width and exposure in chemical during lift-off process on the flatness of transconductance (Gm) curves. In the first group, two different gate recess etch times were used. The exposure in chemical during liftoff process was long. In the second group, two wafers were etched at a fixed time but the exposures in lift-off process chemical were different. In the final group, 3 wafers were etched for three different intermediate times and the exposure in lift-off process chemical was short.

Figure 1 show the plots of Gm versus gate bias (Vgs) at drain source voltage (Vds) of about 3.5 V for the wafers with two different recess etch times. The Gm curves of the devices are not flat. The reduction of Gm from the peak to 0.75 V of Vgs was found to be 20 ms/mm for the devices with shorter etch time. This is less than the reduction of 28 ms/mm for the devices with longer etches. The longer ungated channel is likely the reason of higher reduction of Gm from the peak value, since the exposure in the liftoff process chemical was same for both wafers.

Figure 2 show the plots of Gm versus Vgs of the wafers with same recess etch time but different exposures in chemical. Here also we noticed that the Gm flatness depends on the duration of exposure in the lift-off process chemical. The Gm of the devices reduced from 168 ms/mm (peak) to 150 ms/mm (at Vgs = 0.75 V). However, when the exposure time is doubled the Gm reduced from 168 ms/mm (peak) to 144 ms/mm (at Vgs = 0.75 V).

The above observations indicate that the gate recess etch time and exposure in chemical have a significant role in determining the Gm flatness. Therefore, in the final experiment the exposure in the chemical was short, and the wafers were etched for three different intermediate times to find out the correct condition for flat Gm curve. Silicon nitride passivation layer was deposited after gate metal liftoff. Figure 3 show the Gm curves of the wafers with three different intermediate recess etch durations and a short exposure in lift-off process chemical. All Gm curves are flat up to around 0.75 V of Vgs, which is likely due to less surface states resulted from the shorter ungated channel than the previous wafers. It is also due to reduction of material etching in the ungated channel for less exposure in chemical. The median breakdown voltages (Vb2) increased from 13 V to 15 V with the increase of recess etch time.

Fifth order polynomial fitting was performed of the Ids vs Vgs transfer characteristics (Fig. 4) to understand the linearity of the devices. Much lower values of the second and third order coefficients (-7 and -5.9) of the devices with short recess etch time indicate better linearity of the devices with flat Gm curves. Finally a push pull amplifier was fabricated using the optimized process. The gain, OIP2 and OIP3 were found to be 20 dB, 81 dBm and 45 dBm, respectively.

[1] A. Y. Tkachenko, D. Bartle, and Ce-Jun Wei, "Correlation between Ungated Recess Width and Linearity of GaAs MESFETs," *Microwave Journal,* pp. 1-8, July 1 1999.

[2] D. Greenberg, L. Del Alamo, R. Bhat “Impact Ionization and Transport in InAlAs/n+ - InP HFET”, *IEEE Trans. Electron Devices*”, Vol 42, No. 9, pp. 1574-1582, 1995.

[3] Y. C. Lin, E. Y. Chang, H. Yamaguchi, W.C Wu, C. Y. Chang, “A δ – doped InGaP/InGaAs pHEMT with different doping profiles for device-linearity improvement” *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1617-1625, July 2007.

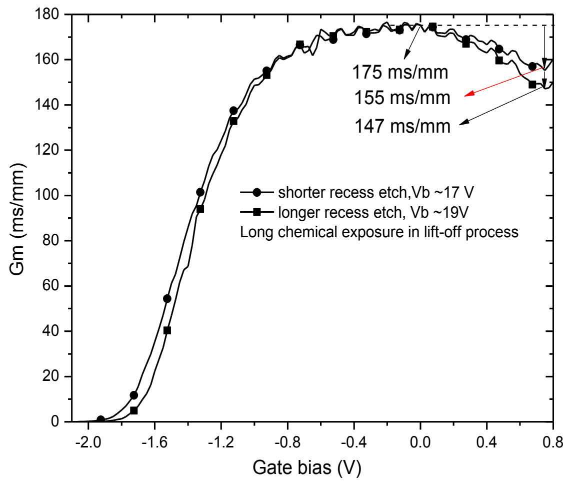

Fig. 1. Plot of Gm versus gate bias obtained at Vds of about 3.5 V for different recess etch durations

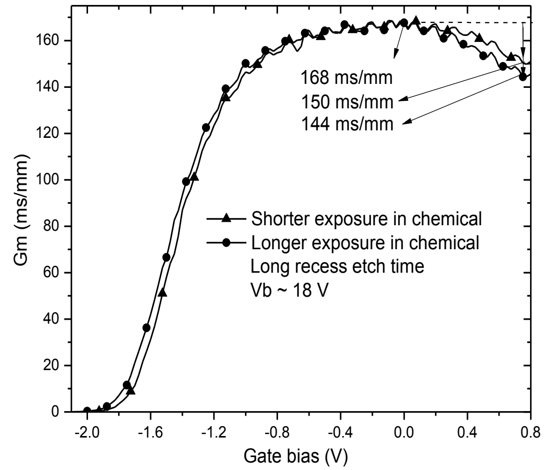

Fig. 2. Plot of Gm versus gate bias obtained at Vds of about 3.5 V for different exposures in chemical

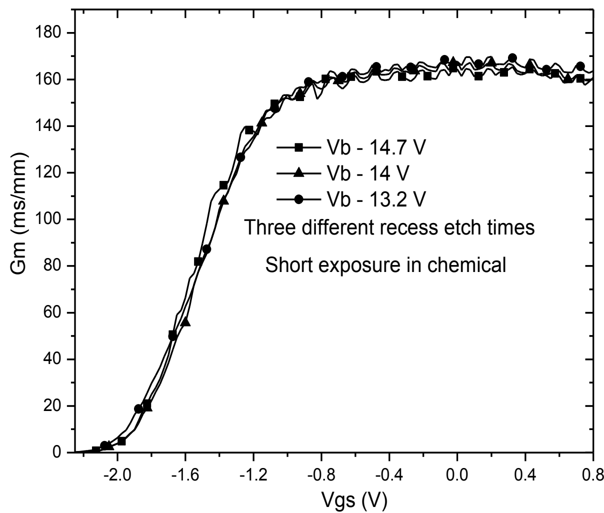

Fig.3. Plot of Gm versus gate bias obtained at Vds of about 3.5 V for three different recess etch times and short exposure in chemical

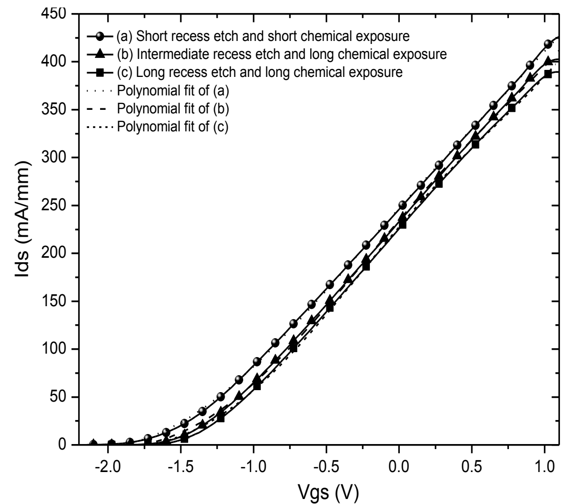

Fig.4. Ids vs Vgs plots with polynomial fitting