Temperature Measurement and Modeling of Low Thermal Resistance GaN-on-Diamond Transistors

J. Pomeroy[a]*, M. Bernardoni[a], D.C. Dumka[b], D.M. Fanning[b], M. Kuball[a]

[a]H.H. Wills Physics Laboratory, University of Bristol, Bristol, BS8 1TL, UK

[b]TriQuint Semiconductor, Inc., 500 W. Renner Road, Richardson, TX, 75080, USA

*James.Pomeroy@bristol.ac.uk

The RF output power density achievable for GaN-based high electron mobility transistors (HEMTs) is limited by thermal resistance, despite the relatively high thermal conductivity of the SiC substrates commonly used (κ_{SiC}=370-490 W/m°C). New thermal management solutions are needed to fully realize the potential of AlGaN/GaN HEMTs in high-power RF applications, particularly in the near-junction region where Joule heating occurs. Replacing SiC substrates with the highest thermal conductivity material available, diamond (κ up to 2000 W/m°C), will result in significantly lower thermal resistance AlGaN/GaN HEMTs. Although the potential thermal resistance benefit of GaN-on-diamond is clear, and excellent RF electrical performance has already been demonstrated, experimental assessment of the thermal resistance of GaN-on-diamond transistors is still needed, to demonstrate the low thermal resistance already achieved and to validate the thermal models that will be used to optimize device design. In this work we combine Raman thermography and thermal simulation to assess the thermal resistance of state-of-the-art GaN-on-diamond HEMTs.

In order to demonstrate the benefit of current GaN-on-diamond we compare peak channel temperatures in GaN-on-diamond and GaN-on-SiC transistors with identical layouts (Fig. 1). Peak channel temperatures, which are extrapolated from Raman measurements with the aid of thermal modeling, were found to be 40% lower in GaN-on-diamond with respect to GaN-on-SiC for device geometry measured. A low thermal resistance of 10 °C mm/W is found for the GaN-on-diamond transistor at a power dissipation of 15 W/mm, for the device geometry considered. GaN-on-diamond thermal resistance will be further reduced by identifying and optimizing any thermal resistance limitations in the heat path between device channel and heat sink. In previous Raman thermography measurements on ungated transistors, diamond thermal conductivity values of up to 1200 W/m°C have been measured close to the GaN/diamond interface and a GaN/diamond interfacial thermal resistance of 2.7±0.3 $\times 10^{-8}$ m^2°C/W was obtained, having a similar magnitude to measured GaN/SiC interface thermal resistances.

The GaN layer, forming the active component of the measured GaN-on-diamond wafer, originates from GaN-on-silicon epitaxy. After removal of the silicon substrate and growth transition layers, a 25 nm-thick dielectric layer is deposited prior to the CVD growth of diamond on the GaN backside. In order to understand the contribution from GaN/diamond interfacial thermal resistance and diamond substrate thermal conductivity to the total device thermal resistance, GaN and diamond temperatures were measured at the centre of two and four finger GaN-on-diamond transistors, illustrated in Figs. 2 and 3. The GaN/diamond interfacial thermal resistance is found to account for about 40% of the total transistor thermal resistance for the device geometry measured, excluding the thermal resistance associated with wafer mounting; decreasing the GaN/diamond interfacial resistance will bring the greatest benefit to current GaN-on-diamond transistors.

Finite element thermal models, including experimentally obtained thermal conductivities, closely match Raman measured temperatures for both the two and four finger transistors (Figs. 2 and 3). By using the experimentally validated transistor thermal model and material parameters, the scaling of thermal resistance with gate pitch and the total number of gate fingers can be investigated, as illustrated in Fig. 4 for GaN-on-diamond and GaN-on-SiC HEMTs. We observe that the high thermal conductivity diamond substrate plays in increasingly important heat spreading role when gate pitch is reduced: A ~2× reduction in thermal resistance is obtained for a 32 finger GaN-on-diamond HEMT with a 10 µm gate pitch, with respect to an equivalent GaN-on-SiC transistor; a 2.5× improvement was attained by replacing the CuW heat spreader with diamond. Low thermal resistance GaN-on-diamond HEMTs will ultimately enable devices with a greatly reduced foot print.

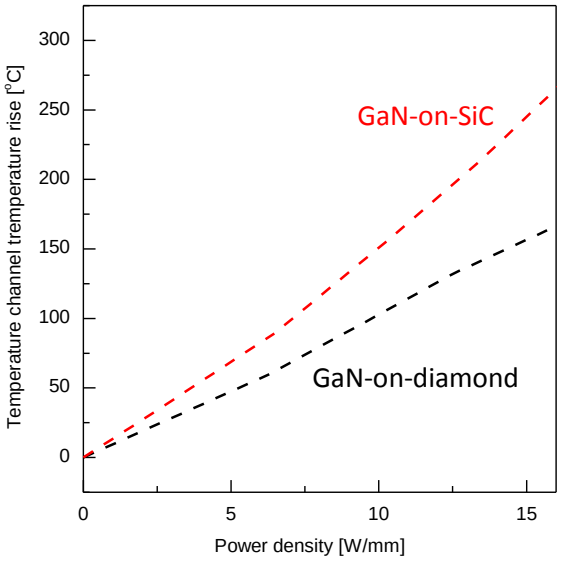

Figure 1: Peak channel temperatures obtained for 2×100 µm, 35 µm gate pitch AlGaN/GaN HEMTs, comparing GaN-on-diamond versus GaN-on-SiC. The GaN-on-diamond transistor exhibits a 40% lower thermal resistance for the measured device geometry. Peak channel temperature was determined from Raman thermography measurements with the aid of thermal modeling.

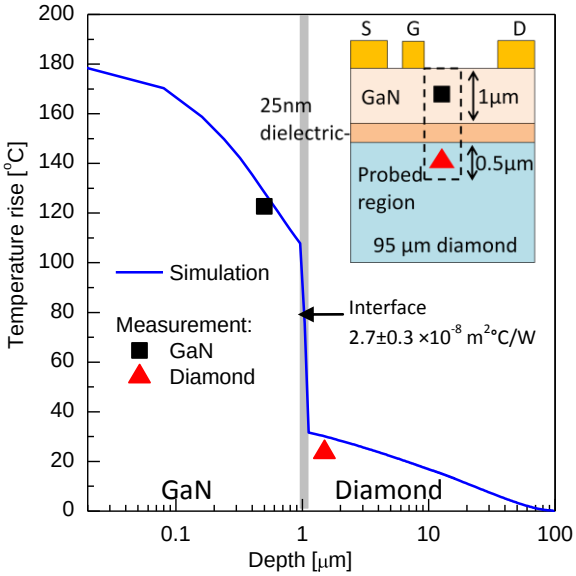

Figure 2: Measured GaN and diamond temperatures for a 2×100 µm, 35 µm gate pitch GaN-on-diamond transistor operated at a 20 V source drain bias and 15.7 W/mm power dissipation. A schematic cross section of area probed in the Raman measurement is shown as an inset. The vertical temperature profile overlaid is generated from a 3-D finite element modeling, using thermal material parameters determined experimentally.

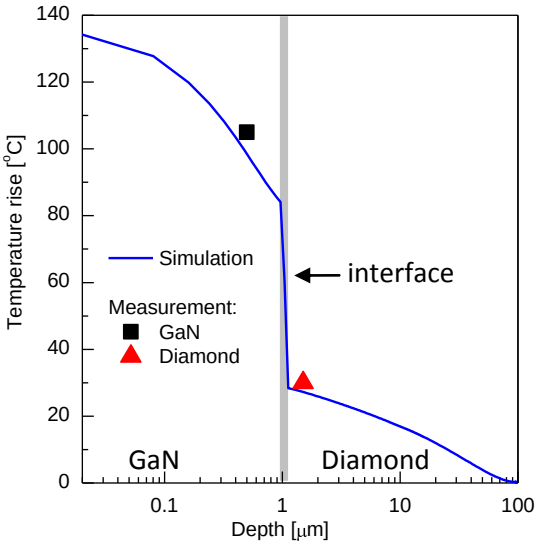

Figure 3: Measured GaN and diamond temperatures for a 4×100 µm, 35 µm gate pitch GaN-on-diamond transistor operated at a 17.5 V source drain bias and 11.4 W/mm power dissipation. The vertical temperature profile overlaid is generated from a 3-D finite element model, using thermal material parameters determined experimentally.

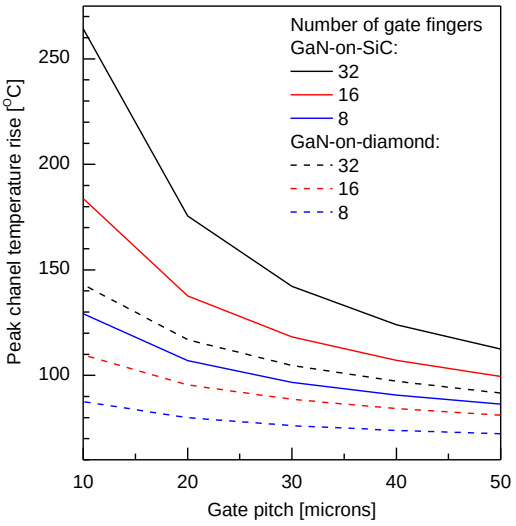

Fig. 4. Simulated GaN HEMT peak channel temperature: GaN-on-SiC versus GaN-on-diamond for varying gate pitch and total number of fingers. Gate width and power dissipation are fixed at 125 µm and 5 W/mm, respectively. Experimentally obtained parameters are used for GaN-on-Diamond ($\kappa_{diamond}$ = 1200 W/m°C, $TBR_{GaN/diamond}$ = 2.7×10^{-8} m^2°C /W). A best case SiC thermal conductivity of 490 W/m°C and a typical GaN/SiC TBR of 1.7×10^{-8} m^2°C/W were used in the GaN-on-SiC model. The model includes a standard AuSn die attach and CuW heat spreader, with a fixed 25°C baseplate temperature.