

# Sputtered Iridium Gate Module for GaN HEMT with Stress Engineering and High Reliability

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## Motivation

AlGaIn/GaN HEMT rf transistors are rapidly developing due to their high output power density, high operation voltage and high input impedance. Ni-based gate metallization is widely used to form the Schottky gate contacts. However, temperature and electric field levels are higher in AlGaIn/GaN compared to traditional III-Vs and therefore the diffusion of Ni into AlGaIn/GaN constitutes a reliability issue [1].

Gold diffusion from the gate head is another source of deterioration for HEMT performance and reliability. It has been found that gold may be diffusing via the gate foot side wall towards the Schottky barrier [2]. The shadowing effect from directional deposition by evaporation prevents full coverage of the Schottky metal in the gate trench and in this way enables sideway diffusion. This in turn not only demands for more resistant Schottky metallisation but also requests hermetic sealing of the Schottky metal interface from diffusion.

Several attempts have been made to replace the Schottky gate metal by more resistant metallization schemes. In particular, refractory metals exhibiting very high melting point are promising candidates [3]. On the other hand, stress in evaporated thin films is rather high for high melting point metals. This and the extreme lateral dimensional ratio of the gate could lead to poor adhesion and roll up of the gate contact. Therefore, stress engineering is highly desirable to promote well adhering Schottky metal in the gate trench.

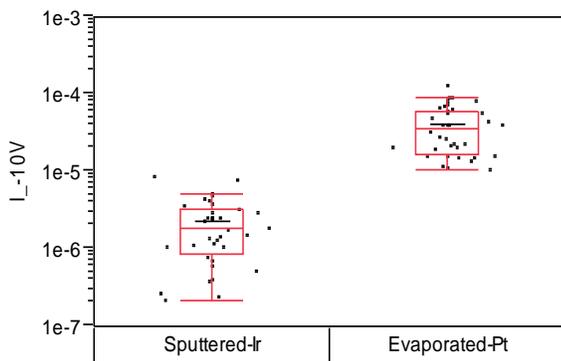


Fig.1 Gate diode reverse leakage  $I_{-10V}$  measured at  $-10V_G$  and RT

## Approach

The metallurgical barrier effect of the Schottky contact metal and hermetic sealing are accomplished by conformal deposition of the Schottky metal over the gate trench and adjacent area. Isotropic deposition methods are required for conformal growth of the Schottky metal. Thus, sputter deposition is the preferred method here. Iridium as a refractory metal with a melting point of 2460°C and simultaneously providing a high work function  $> 5$  eV is a prime candidate.

The deposition of a conformal metal layer requires an isotropic deposition method. Such methods are not compatible with traditional lift-off as a masking technique. Particularly, lift-off technologies require strict anisotropic deposition. Therefore, forming of the Schottky contact electrode has been changed from an additive structuring method, i.e. lift-off, to subtractive structuring.

Refractory metals tend to build rigid layers due to their high mechanical elastic modulus. This is beneficial for a metallurgical barrier but may adversely effect performance when mechanical stress during film growth is not properly managed and may even lead to delamination of the film. Sputtering technology typically yields compressive metal films but by choosing appropriate plasma parameter stress can be adjusted from compressive to tensile. Here, iridium films are adjusted to stress levels much lower than 100 MPa.

Both, RF-power as well as high voltage switching applications suffer from electronic traps that are responsible for poor performance under dynamic operation. Trap generation in the vicinity of the gate contact due to energetic particles from the sputter plasma has to be avoided by choosing suitable processing parameter. RF-data will be chosen as a benchmark of this technology against the evaporated standard.

## Results

Here, we report data collected for the experiments performed on identically processed GaN-on-SiC devices, except for the gate metallisation module.

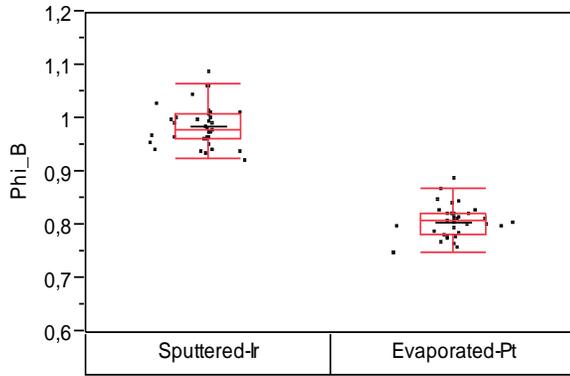


Fig.2 Gate diode barrier height  $\Phi_B$  (eV)

The gate length is 0.25  $\mu\text{m}$ . Sputtered iridium gate metallisation is compared with evaporated platinum. Comparison of the dc data from the 2 metallisation schemes shows only minor differences for gm (240 mS/mm) and pinch-off (-3.2 V).  $I_{D\text{Smax}}$  is 700 mA/mm for iridium and 770 mA/mm for platinum. There are remarkable differences in leakage currents as shown for the gate diode reverse bias (Fig.1). For the sputtered iridium leakage is slightly above  $10^{-6}$  A whereas evaporated platinum is more than a decade higher. Also, a difference in barrier height is observed (Fig.2). Since the work function of both materials is very close (5.5-5.8 eV) the different stress levels of the metal films may come into consideration. Annealing studies that generate different stress pattern support this argumentation.

Step-stress-tests were performed under high temperature reverse bias condition (HTRB) at -5 V<sub>G</sub> and 150°C (Fig.3). Both gate modules show stable operation up to the highest drain voltage of 100 V. Similar to the results of Fig.1 the level of leakage is more than a decade higher for evaporated platinum. Also a pronounced ripple is visible here that could indicate trapping effects.

S-Parameter are compared for the 2 gate modules.

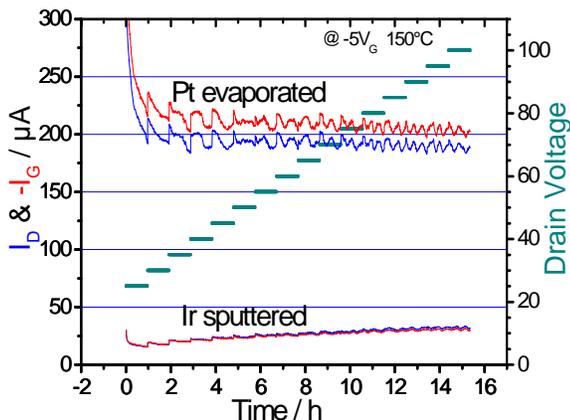


Fig.3 Step-Stress-Test under high temperature reverse bias condition (HTRB)

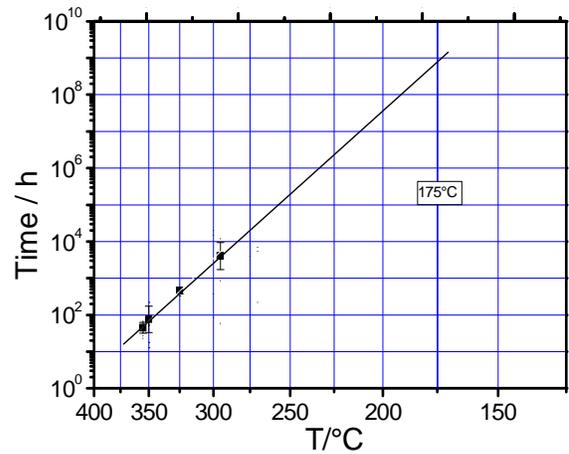


Fig.4 Arrhenius plot of sputter deposited Iridium gate module

Small signal operation at a bias of 40 V, 50 mA/mm is performed for devices of 0.1 mm total gate width and MAG values are extracted for the frequencies of 2, 10 and 18 GHz. For sputtered iridium devices at these frequencies the MAG values are 22.7, 15.5 and 11.5 dB and the corresponding data for evaporated platinum are 22.2, 15.1 and 11.3 dB showing minor differences only.

Load pull data are taken on devices having a total gate width of 1 mm and are operated at 50 V<sub>D</sub>, and 2 GHz. Large signal gain G<sub>t</sub> is in the range 26.5±0.5 dB for both deposition methods. RF-power for iridium sputtered devices yields 4.8 W/mm, whereas evaporated Pt shows a slightly higher power density of 5.9 W/mm which in part is due to slight differences in sheet resistance. The power added efficiency is of huge importance not only for optimum design of amplifier but here also serves as an indicator of additional traps initiated by the sputtering process during metal deposition. PAE ranges here from 59 - 61 % for both deposition methods, showing no difference between both types. It is revealing that deposition conditions for sputtering can be chosen in an appropriate way for gate metal deposition.

Lifetime of devices was assessed by thermally accelerated testing using the Arrhenius method and tests were performed in the range 290-355°C. The extrapolated lifetime for a channel temperature of 175°C is > 10<sup>8</sup> hours. The resulting activation energy is 2.0 eV (Fig.4).

#### References

1. Miura N, Nanjo T, Suita M, Oishi T, Abe Y, Ozeki T, et al. Solid State Electron 48-689(2004).
2. Jung H, Behtash R, Thorpe J, Riepe K, Bourgeois F, Blanck H, et al. Phys Stat Solid C6-976(2009).
3. Würfl J, Hilsenbeck J, Nebauer E, Tränkle G, Obloh H, Österle W. Microelectron Reliab 40-1689(2000).