

Effects of Field Plate and Epitaxial Wafer on AlGaIn/GaN HEMTs with Active Harmonic Tuning

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Abstract

We report on the influences of AlGaIn/GaN epitaxial wafers and device structures on drain efficiency using a third harmonic tuning active loadpull system. Device fabricated on epitaxial wafer of low-density trap state can achieve high drain efficiency. In addition, as the length of the device's source field plate is reduced, its drain efficiency increases. We have demonstrated that a device without source field plate fabricated on this type of wafer can achieve a drain efficiency of 84%.

INTRODUCTION

AlGaIn/GaN HEMTs devices are studied intensively for applications such as high power microwave devices used in satellite communication systems and fixed wireless access systems. One of the most important issues with these applications is efficiency. In recent years, with the progress of harmonic-tuned amplifiers such as Class E, F and J amplifiers, high efficiency performance can be achieved with GaN devices [1][2][3]. A packaged high power FET device was demonstrated with internal harmonic matching circuit [4].

Efficiency of the device is greatly affected by the current-collapse phenomenon [5] which can be generally prevented by employing a source field plate in the device. In this paper, we report on the effects of epitaxial wafers and device structures on a device's drain efficiency. The devices were evaluated using a third harmonic tuning active loadpull system.

EXPERIMENT

Two kinds of AlGaIn/GaN epitaxial wafers were used in this study, named as "Epi wafer A" and "Epi wafer B". The wafers were grown on SI SiC substrates by MOCVD with a difference in the GaN buffer layer. Before the device fabrication, epitaxial wafers were determined by photoluminescence with 325nm He-Cd laser.

Three device structures as shown in figure 1 were fabricated on both wafers, they were (a) without source field plate, (b) with source field plate $L_{sfp}=0.5\mu\text{m}$ and (c) $L_{sfp}=1.5\mu\text{m}$. All devices have the same gate length (L_g) of

$0.6\mu\text{m}$ and a total gate width of $540\mu\text{m}$ ($270\mu\text{m} \times 2$). A curve tracer was used to evaluate the DC current collapse of the devices and a harmonic tuning active loadpull system used to determine their drain efficiency. Figure 2 illustrates the block diagram of the loadpull system which comprises of third harmonic active tuners. The devices biased at 40V drain supply were evaluated at a fundamental frequency (f_0) of 3.0 GHz.

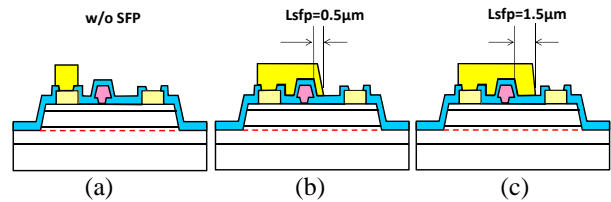


Figure 1 Device Structure (a) without source field plate, (b) with Source field plate $L_{sfp}=0.5\mu\text{m}$ (c) $L_{sfp}=1.5\mu\text{m}$

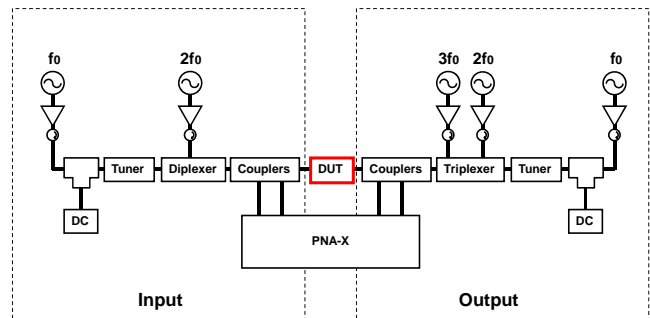


Figure 2 Schematic Harmonic tuning Load-pull systems

RESULTS AND DISCUSSION

Figure 3 shows the measured photo-luminescence spectrums of the two wafers where yellow luminescence (YL) can be seen in “Epi wafer A”, implying that it has a considerable high-density trap states. In contrast, “Epi wafer B” has low trap density.

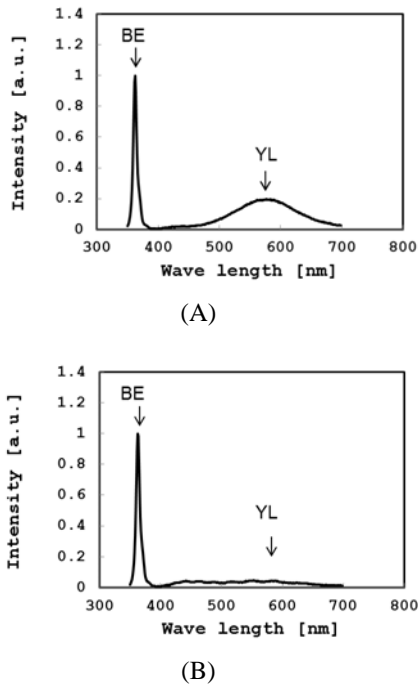


Figure 3 Photo-Luminescence of (A) Epi wafer A (B) Epi wafer B.

The drain current-voltage characteristics of devices on both epi-wafers are as shown in figure 4. The gate voltages were applied from +1V to -4V with a step of 1V. The red color curve shows the current characteristics swept to a maximum drain voltage of 10V and the blue curve to 100V. Current collapses phenomenon can be seen at devices fabricated on “Epi wafer A” and with a slight improvement for devices with source field plate. In contrast, current collapses were not prominent in low-density trap state “Epi wafer B”.

Figure 5 shows the measured drain efficiency of the devices. For devices fabricated on “Epi wafer A” which has high-density trap states, it can be seen that the drain efficiency increases with longer source field plate. This can be attributed to the reduction in gain at the second- and third-harmonic frequencies ($2f_0=6\text{GHz}$, $3f_0=9\text{GHz}$) when the source field plate length is increased. In contrast, device fabricated on “Epi wafer B” which has low-density trap state has higher drain efficiency as the source field plate length is

reduced. With “Epi wafer B”, a device without source field plate can achieve an efficiency of 84% which is about 20% higher than that of “Epi wafer A”. It also delivers an output power of 2.8W.

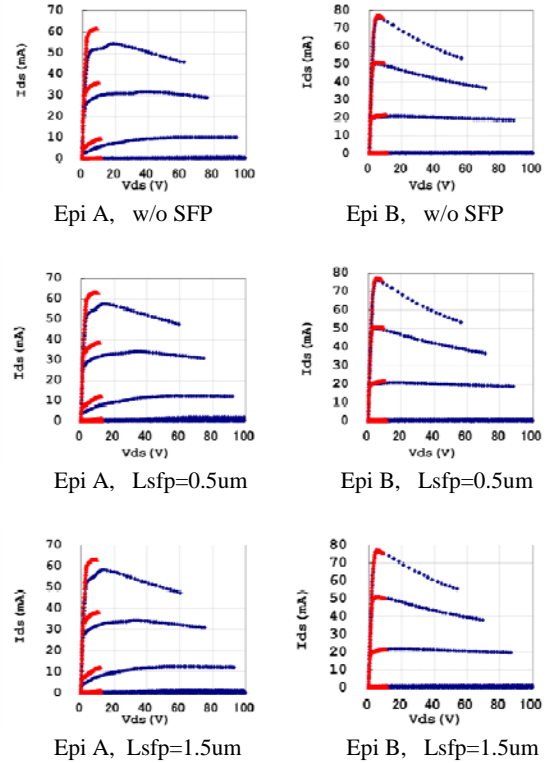


Figure 4 The drain current-voltage characteristics of 100μm. Drain bias swept from 10V, 100V. The gate bias is applied from $V_{gs}=+1\text{V}$ to -4V and step is 1V.

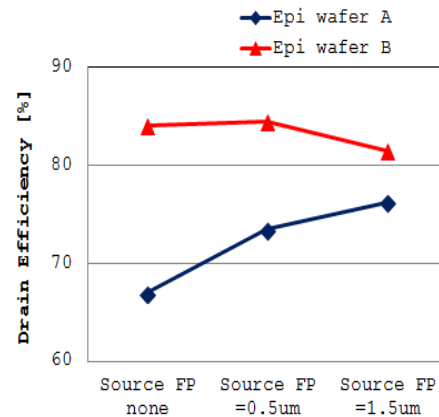


Figure 5 Dependency of drain efficiency on wafer and device structure using the third harmonic tuned loadpull. The devices biased at 40V drain supply

CONCLUSIONS

In this study, we have shown that low-density trap epitaxial wafer is crucial to a GaN device performance. Device fabricated on this type of wafer has minimal current collapse phenomenon which does not require a source field plate to improve its efficiency. We have demonstrated such a device achieving a drain efficiency of 84%.

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ACRONYMS

HEMT: High Electron Mobility Transistor
BE: Band Edge
YL: Yellow Luminescence

