Need for Defects in Floating-Buffer AlGaN/GaN HEMTs

M. J. Uren[1], M. Silvestri[1], M. Cäsar[1], J.W. Pomeroy[1], G.A.M. Hurkx[2], J.A. Croon[3], J. Šonský[2], and M. Kuball[1]

[1]CDTR, H H Wills Physics Department, University of Bristol, BS8 1TL, UK. Michael.Uren@bristol.ac.uk
[2]NXP Semiconductors Research, Kapeldreef 75, 3001 Leuven, Belgium
[3]NXP Semiconductors Research, 5656 AA Eindhoven, The Netherlands

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Abstract

Carbon is a deep-level p-type acceptor in GaN and is used successfully in high-voltage AlGaN/GaN HEMT processes to generate a semi-insulating buffer for off-state leakage and breakdown suppression. However, p-type doping has also been linked to dynamic R_{ON} dispersion and current-collapse (CC) due to the absence of an Ohmic contact to the floating GaN buffer region. We demonstrate that current-collapse free C-doped HEMTs can be realized using epitaxial defects which short the floating buffer to the 2DEG.

INTRODUCTION

GaN HEMTs are ideally suited for high-efficiency high-frequency power switching applications, aiming to exploit the intrinsic high-voltage, low on-resistance, and low capacitance of this materials system. However issues remain surrounding the problem of dynamic R_{ON} dispersion, otherwise known as current-collapse (CC). This effect manifests itself as an increase in channel resistance following switching the device from the OFF to the ON state, which only returns to the static R_{ON} value after an extended period. CC is the result of transient charge storage in traps, either at the AlGaN surface which exchange charge with the gate contact and form a "virtual gate", or by exchange of charge between the 2DEG channel and the GaN buffer[1]. Virtual gate effects can be effectively controlled using field plates and surface passivation[2], and here we are purely concerned with buffer induced CC.

Power GaN/AlGaN HEMTs require a semi-insulating GaN buffer to prevent OFF state leakage, and this is frequently achieved using carbon doping, resulting in excellent leakage and breakdown performance but with varying reports of CC[3, 4]. Carbon has a complex range of deep levels in the gap, but the most important is an acceptor 0.9eV above the valence band[5]. This means that the buffer is weakly p-type and isolated from the 2DEG at the GaN/AlGaN interface by a depletion region. Simulation has shown that under transient conditions dramatic CC is predicted as a result of back-gating by a negative bias in the floating buffer [6]. Very recently we have demonstrated that this does not normally arise in practice because of leakage along threading dislocations which partially short the floating buffer to the 2DEG[7]. In this paper we extend this work to demonstrate the impact of those dislocations on the full simulated transistor characteristic and show that CC can be significantly reduced by their presence.

EXPERIMENT

AlGaN/GaN HEMT devices taken from a GaN on silicon power switching process development were investigated. Example device performance was reported in [8]. These devices had gate and source connected field plates to effectively suppress surface related CC. Two different wafers have been compared, but with identical C-doped GaN on Si epitaxy. The epitaxy used an undoped channel region, a carbon doped GaN buffer, strain relief layers, all grown on p-type Si. Devices from the two wafers were very similar under DC operation but Wafer A showed moderate CC, whereas Wafer B was essentially CC free. Fig. 1 shows a dynamic *I-V* analysis (DIVA) measurement from either the ON state or the OFF state illustrating the difference. Fig. 2a shows a conventional dynamic R_{ON} measurement and demonstrates the long time constant required for recovery following switching from OFF to ON, again showing the strong difference between the wafers.

Pulsed substrate bias measurements were used to exclude any possibility of surface trapping effects as shown in Fig. 2b [9, 10]. The observation of a similar time constant and

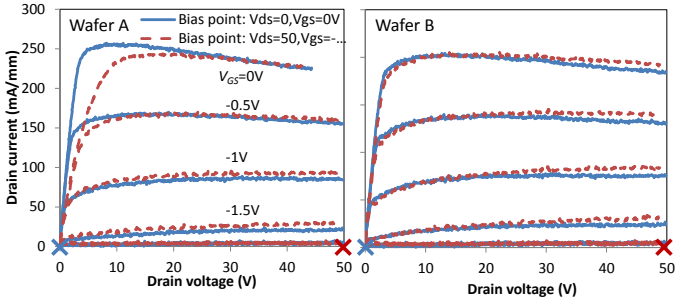

Fig. 1: Double pulse (DIVA) measurement of AlGaN/GaN HEMTs from ON (blue lines V_{DS}=0,V_{GS}=0V) and OFF (red dashed lines V_{DS}=50,V_{GS}=-3V) quiescent bias points. Pulse durations 1µs/1ms, V_{GS}=0,-0.5 … -2.0V. Wafer A shows moderate current-collapse, whereas Wafer B is almost ideal.

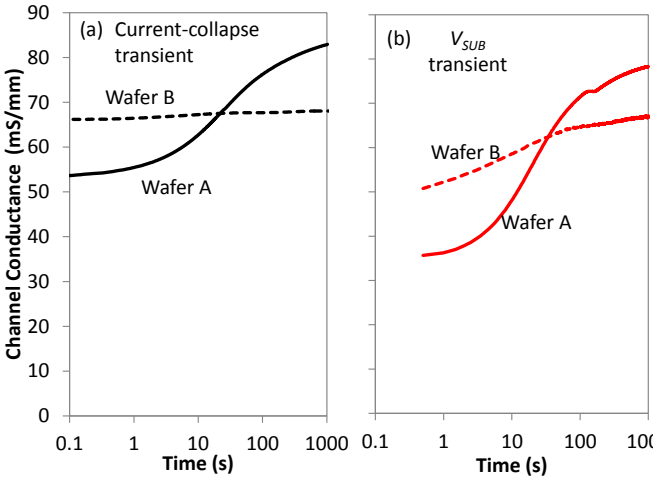

Fig. 2: Drain current transients (a) following step from OFF state (V_{DS}=50V, V_{GS}=-3V) to ON state (V_{DS}=1V, V_{GS}=0V), (b) following step from V_{SUB}=0 to −200V with V_{DS}=1V. Similar time-constant and wafer dependence is observed indicating a common transient origin.

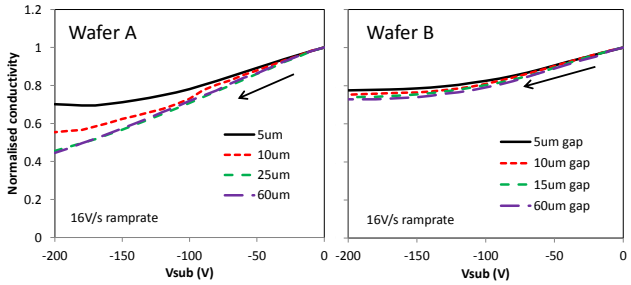

Fig. 3: Normalised sheet conductivity of ungated structures of varying gap size as V_{SUB} is swept from 0 to −200V.

wafer dependence to that seen in Fig. 2a clearly demonstrates that buffer related and not surface related CC is dominant in these devices.

Ramping the substrate bias allows the location and nature of the traps to be determined as described in [7]. Fig. 3 shows that at small V_{SUB}, wafer B showed capacitive coupling between the 2DEG and the Si substrate indicated by a constant dI/dV_{SUB}, but then showed a saturation in current at higher $|V_{SUB}|$ values. This requires the accumulation of positive charge in the buffer, and indicates that the potential in the buffer was pinned by leakage through the reverse biased P-N (buffer to 2DEG) junction once the vertical applied electric field exceeded a critical value. Varying the source-drain gap proved that for Wafer B the leakage occurred over the entire surface, whereas for Wafer A there was strong leakage only under the contacts.

MODEL

GaN on Si is highly defective with typically >10^9cm^{-2} dislocations, and it is those defects which have been identified as the source of reverse leakage in GaN LEDs[11]. Those threading dislocations act as trap assisted tunneling

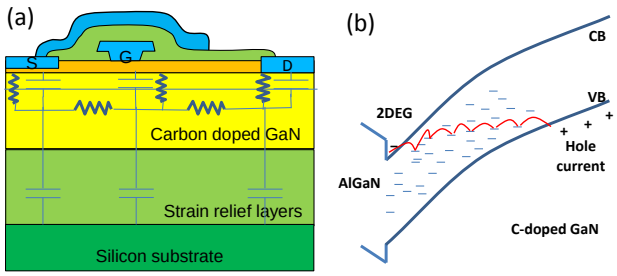

Fig. 4: (a) Schematic showing the vertical and lateral leakage and capacitive paths important in these GaN HEMTs. (b) Trap assisted tunneling process along a dislocation to inject holes from the 2DEG into the buffer during swept V_{SUB} measurement.

paths allowing the injection of holes into the buffer from the 2DEG as shown in Fig 4b[12]. Fig. 4a illustrates the equivalent circuit which is required to explain the substrate bias sweep measurements shown in Fig. 3, with capacitive coupling between the layers combined with TAT leakage and lateral hopping between C-doped trap sites. The different leakage paths between wafers A and B likely arose from differences in the fabrication process electrically activating/deactivating mixed and screw dislocations. This resulted in the suppression of vertical leakage in the region between the contacts in Wafer A[7].

SIMULATION

To test the impact of these threading dislocation paths on CC, device simulations were undertaken to try and reproduce the DIVA measurements shown in Fig. 1 using the methodology described in [6]. Sets of 130 transient simulations from either the ON state of V_{DS}=0V, V_{GS}=0V or the OFF state at V_{DS}=50V, V_{GS}=-3V to V_{DS}, V_{GS} points covering the entire I_D-V_{DS} plane were undertaken. Each transient ramp was carried out in 1ns and the current was recorded 1µs after the ramp. The GaN resistivity and C acceptor level 0.92eV above the valence band were determined experimentally by dynamic transconductance[7, 13] and so an active carbon density of 2x10^{18}cm^{-3} was used in the simulation. Simulating the effect of a distributed set of

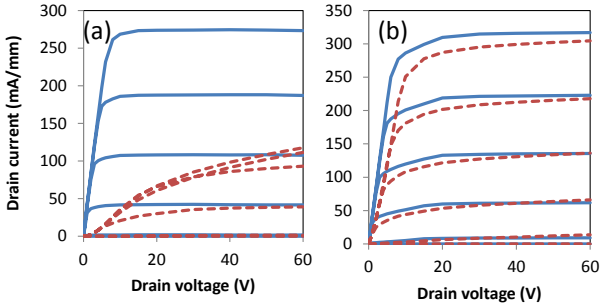

Fig. 5: Simulated double pulse (DIVA) measurements for the same conditions as in Fig. 1. (a) floating p−type buffer, whereas (b) has a P++ shorting region to the GaN buffer under the source and drain.

leakage paths as occurred in Wafer B was not currently feasible, however simulating Wafer A with its leaky contacts to the p-type buffer was straightforwardly achieved by including a small P++ doped region under the source and drain contacts. This simulation of Wafer A was then compared with a fully floating C-doped buffer and the results are shown in Fig. 5.

The floating p-type buffer resulted in an extreme CC as can be seen in Fig. 5a, whereas adding a short only under the contacts reproduced the moderate CC behavior of Wafer A (Fig. 5b). The floating buffer allowed the entire OFF state V_{DS} to be dropped across a depletion region under the drain resulting in back gating of the entire gate-drain gap, and a huge increase in ON-resistance. By contrast, the leakage path under the drain (Fig. 5b, Wafer A) prevented the formation of this deleterious space charge region. However space charge still accumulated in the buffer region in between the contacts resulting in the moderate CC apparent in Fig. 5b. In the case of wafer B, leakage paths existed across the entire source-drain gap, so the build-up of space charge was suppressed along the entire channel, resulting in the excellent CC performance seen in Fig. 1b.

CONCLUSIONS

C-doped buffers can deliver low current collapse, however fabrication processes must ensure that they do not suppress defect-induced leakage. Contrary to normal expectations, vertically conducting defects are essential for the functioning of lateral GaN-on-Si power devices using C-doped buffers. The leakage paths provide a route to tie the potential of the GaN buffer to the 2DEG, suppressing back-gating induced current-collapse.

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REFERENCES

[1] S. C. Binari, P. B. Klein, and T. E. Kazior, *Proc. IEEE,* vol. 90, pp. 1048-1058, 2002.
[2] Y. F. Wu, *et al*., *IEEE Elec. Dev. Lett.,* vol. 25, pp. 117-119, Mar 2004.
[3] E. Bahat-Treidel, *et al.*, *IEEE Trans. Elec. Dev.,* vol. 57, pp. 3050-3058, Nov 2010.
[4] C. Poblenz, *et al.*, *J. Vac. Sci. Technol.,* vol. B22, p. 1145, 2004.
[5] J. L. Lyons, A. Janotti, and C. G. Van de Walle, *Appl. Phys. Lett.,* vol. 97, p. 152108, 2010.
[6] M. J. Uren, J. Möreke, and M. Kuball, *IEEE Trans. Elec. Dev.,* vol. 59, pp. 3327-3333, 2012.
[7] M. J. Uren, *et al*., *IEEE Elec. Dev. Lett*., vol. in press, 2014.
[8] J. J. T. M. Donkers, *et al.*, CS-MANTECH, New Orleans, pp. 259-262, 2013.
[9] M. Marso, *et al., Appl. Phys. Lett.,* vol. 82, pp. 633-635, Jan 27 2003.
[10] C. H. Zhou, *et al*., *IEEE Elec. Dev. Lett.,* vol. 33, pp. 1132-1134, Aug 2012.
[11] D. S. Li, *et al., J. Appl. Phys.,* vol. 96, pp. 1111-1114, Jul 2004.
[12] Q. F. Shan, *et al., Appl. Phys. Lett.,* vol. 99, p. 253506, Dec 2011.
[13] M. Silvestri, M. J. Uren, and M. Kuball, *Appl. Phys. Lett.,* vol. 102, p. 073501, Feb 2013.

ACRONYMS

2DEG: 2 Dimensional Electron Gas
C: Carbon
CC: Current-Collapse
DIVA: Dynamic Current-Voltage Analysis
HEMT: High Electron Mobility Transistor
TAT: Trap Assisted Tunneling