

Comparative Study of AlGaN/GaN HEMTs with LPCVD- and PECVD-SiN_x Passivation

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Keywords: AlGaN/GaN HEMTs, current collapse, passivation, LPCVD, PECVD, SiN_x.

Abstract

LPCVD technique is utilized for growth of SiN_x passivation of AlGaN/GaN HEMTs. Compared with conventional PECVD-SiN_x passivation, effective current collapse suppression and remarkably improved RF power performance are achieved by LPCVD-SiN_x passivation. The improved passivation by LPCVD-SiN_x is confirmed by a significantly reduced lateral SiN_x/AlGaN interface leakage current via interface traps (compared to PECVD-SiN_x). TEM-EDS analysis of SiN_x/AlGaN interface suggests that the interface traps is originated from the oxidation of the AlGaN barrier layer surface, which is in relation to the fabrication process.

INTRODUCTION

AlGaN/GaN HEMTs have shown great promise as the key components in RF/microwave power amplifiers because of the polarization-induced high mobility as well as density 2-D electron gases and high breakdown E -field [1]. However, AlGaN/GaN HEMTs typically feature a channel with a short distance (e.g., ~20 nm) from the polarized surface, and could easily suffer from surface-state-related adverse effects such as current collapse [2, 3].

To suppress the current collapse, plasma-enhanced chemical-vapor-deposited (PECVD) SiN_x layer is generally adopted to passivate the surface states, except for the recently developed AlN passivation featuring charge-compensation concept [4]. There are several challenging issues for PECVD-SiN_x passivation, including: 1) relative low film quality due to low growth temperature (below 350 °C); 2) possible inherent plasma induced damages to the surface before depositing. In this regards, low-pressure chemical vapor deposition (LPCVD) are most appealing technique for growth of high quality SiN_x passivation layer for AlGaN/GaN HEMTs by virtue of its high growing temperature (typically at above 600 °C) and non-plasma-activated sources [5]. In addition, LPCVD-SiN_x is mature technology in CMOS fabs, which is very attractive for mass production of AlGaN/GaN HEMTs in CMOS line to reduce its fabrication cost.

In this work, CMOS-standard LPCVD-SiN_x layer is successfully demonstrated in the passivation of AlGaN/GaN HEMTs. Compared with conventional PECVD-SiN_x

passivation, effective current collapse suppression and remarkably improved RF power performance are achieved.

DEVICE STRUCTURE AND FABRICATION

The AlGaN/GaN heterostructure used in this work consists of a 24-nm undoped Al_{0.2}Ga_{0.8}N barrier, a 1-nm AlN interface enhancement layer, and a composite Al_{0.02}Ga_{0.98}N/GaN (0.8 μm/0.8 μm) buffer layer. A 120-nm LPCVD-SiN_x passivation layer was deposited on the fresh epilayer at 780 °C and a low pressure of 300 mTorr just after a standard RCA cleaning process. After dry etching openings of the LPCVD-SiN_x layer, ohmic contacts were formed with a Ti/Al/Ni/Au metal stack annealed at 850 °C for 50 s in N₂ ambient. The contact resistance is measured to be 0.85 Ω · mm. Then device isolation is conducted by boron ion implantation. T-shape gate electrode is fabricated after gate opening, followed by a post-gate annealing at 350 °C for 5 min. For the referenced PECVD-SiN_x-passivated GaN HEMTs, RCA wet cleaning is also utilized for cleaning the fresh epilayer, and an extra NH₄OH solution and a 1-min *in-situ* N₂ plasma pretreatment were adopted before PECVD-SiN_x deposition. The gate length (L_G), gate-to-drain distance (L_{GD}), gate-to-source distance (L_{GS}), and gate width (W_G) are 1, 2.75, 1.5 and 2 × 50 μm, respectively.

RESULTS AND DISCUSSION

Transfer characteristics of both LPCVD-SiN_x and PECVD-SiN_x passivated AlGaN/GaN HEMTs are compared and shown in Fig. 1(a). The former features significantly higher drain current density at high gate bias and higher peak extrinsic transconductance than the latter. Moreover, the output power at 3 dB compression point and associated PAE of LPCVD-SiN_x passivated samples, measured at 4 GHz

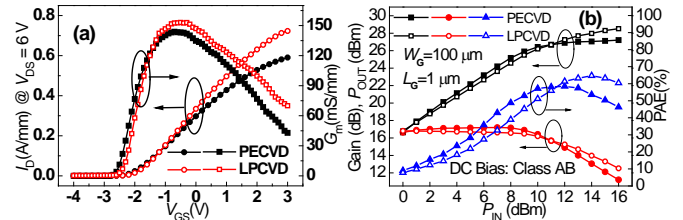


Fig. 1. (a) Transfer characteristics and (b) RF power performance of PECVD-SiN_x and LPCVD-SiN_x passivated AlGaN/GaN HEMTs measured at 4 GHz.

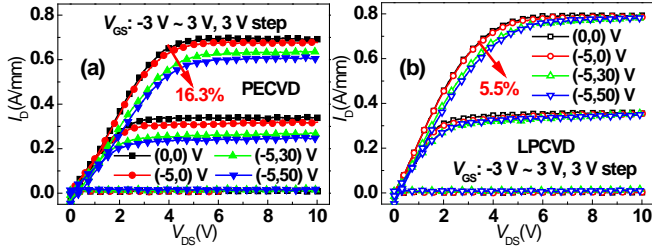


Fig. 2. Pulsed I - V characteristics of (a) PECVD-Si $_x$ and (b) LPCVD-Si $_x$ passivated AlGaIn/GaN HEMTs, measured at different quiescent bias: (V_{GS} , V_{DS}). The pulse width and period are 1 μ s and 1 ms, respectively.

with $V_{DS} = 30$ V, are 6.8 W/mm and 63.2%, respectively, which are 1.8 W/mm and 9.6% higher than that of the PECVD-Si $_x$ passivated ones (Fig. 1(b)).

The effectiveness of LPCVD-Si $_x$ passivation is also demonstrated by pulse I - V characterization, as shown in Fig. 2. As compared with the PECVD-Si $_x$ -passivated samples, the collapse ratio of the LPCVD-Si $_x$ -passivated ones is much smaller even at a high drain bias stress of 50 V. The gate-lag shows nearly no difference in the threshold voltage shift, with only a different decrease in transconductance for both samples (not shown). It suggests that surface-related traps are the dominant cause for the current collapse [6].

Double gate structures with gate-to-gate distance (L_{GG}) ranging from 2.75 to 5 μ m, is introduced to distinguish lateral surface leakage current (I_{SURF}) via Si $_x$ /AlGaIn interface from vertical leakage current (I_{BULK}). The I_{SURF} in PECVD-Si $_x$ -passivated HEMTs increases as L_{GG} decreases, while that for the LPCVD-Si $_x$ passivated ones is much lower and keeps constant for all the L_{GG} (Fig. 3(a)). 2D-VRH assisted by high-density interface states is considered as a possible cause for I_{SURF} [7], which indicates that the traps at LPCVD-Si $_x$ /AlGaIn is much lower than that of PECVD-Si $_x$. The higher I_{BULK} in the LPCVD-Si $_x$ passivated HEMTs further confirms the effective mitigation of ‘virtual gate’ formed by interface traps (Fig. 3(b)).

TEM-EDS mapping of the passivation/AlGaIn interface is adopted to reveal the origin of the interface traps, as shown in Fig. 4. The LPCVD passivated ones show remarkably lower interface oxygen contamination than that of PECVD-Si $_x$ passivated interface. It is thus verified that the surface traps are probably originated from oxygen-related bonds such as Ga-O [8].

CONCLUSIONS

CMOS-standard LPCVD-Si $_x$ is utilized for passivation of AlGaIn/GaN HEMTs. Effective current collapse suppression and RF power performance improvement are achieved. It is verified that it is the oxidation of Si $_x$ /AlGaIn interface that brings about surface traps and contributes to a high lateral surface leakage current through PECVD-Si $_x$ /AlGaIn interface.

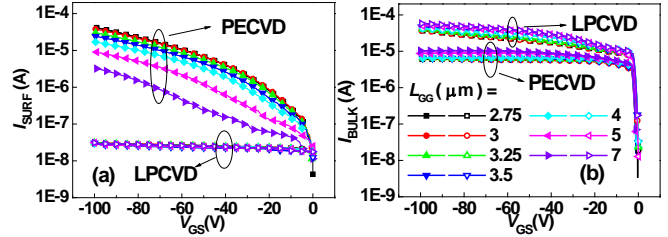


Fig. 3. (a) I_{SURF} - V_{GS} and (b) I_{BULK} - V_{GS} characteristics of PECVD-Si $_x$ and LPCVD-Si $_x$ passivated samples with various L_{GG} .

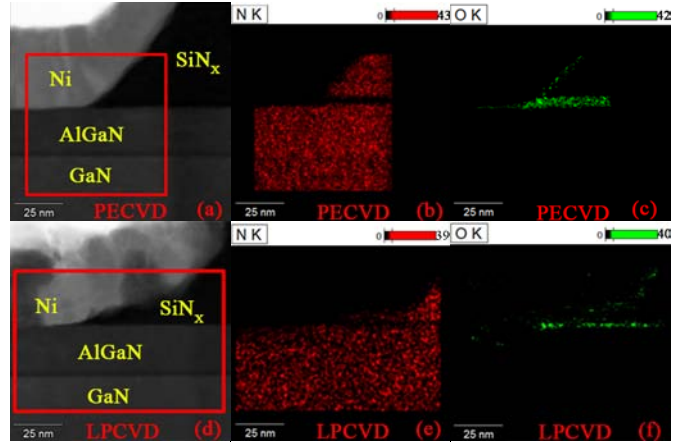


Fig. 4. Element distribution of Si $_x$ /AlGaIn interfaces analyzed by TEM-EDS mapping (in red pane). PECVD/LPCVD: (a)/(d) cross-sectional view, (b)/(e) nitrogen, (c)/(f) oxygen

REFERENCES

- [1] Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, *IEEE Electron Device Lett.* 25, 117 (2004).
- [2] G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, *IEEE Trans. Electron Devices* 50, 886 (2003).
- [3] S. Huang, Q. Jiang, S. Yang, C. Zhou, and K. J. Chen, *IEEE Electron Device Lett.* 33, 516 (2012).
- [4] K. J. Chen and S. Huang, *Semicond. Sci. Technol.* 28, 074015 (2013).
- [5] J. Yota, J. Hander, and A. A. Saleh, *J. Vac. Sci. Technol. A* 18, 372 (2000).
- [6] G. Meneghesso, F. Zanon, M. J. Uren, and E. Zanoni, *IEEE Electron Device Lett.* 30, 100 (2009).
- [7] J. Kotani, M. Tajima, S. Kasai, and T. Hashizume, *Appl. Phys. Lett.* 91, 093501 (2007).
- [8] S. Yang, Z. Tang, K.-Y. Wong, Y.-S. Lin, Y. Lu, S. Huang, and K. J. Chen, *Mapping of interface traps in high-performance Al₂O₃/AlGaIn/GaN MIS-heterostructures using frequency- and temperature-dependent C-V techniques*, 2013 IEEE International Electron Devices Meeting, pp. 6.3.1-6.3.4, December 2013

ACRONYMS

- LPCVD: Low-Pressure Chemical Vapor Deposition
- PECVD: Plasma-Enhanced Chemical Vapor Deposition
- RSD: Reactive Sputtering Deposition
- HEMT: High Electron Mobility Transistor
- TEM: Transmission Electron Microscope
- EDS: Energy Dispersive Spectrometer
- PAE: Power-Added Efficiency
- 2D-VRH: Two-Dimensional Variable Range Hopping