0.15μm GaN MMIC Manufacturing Technology for 2-50 GHz Power Applications

Sabyasachi Nayak, Ming-Yih Kao, Hua-Tang Chen, Trish Smith, Peter Goeller, Weixiang Gao,
Jose Jimenez, Shuoqi Chen, Charles Campbell, Gergana Drandova, and Robert Kraft

TriQuint Semiconductor, 500 W Renner Road, Richardson, TX 75080-1324
Phone: (972) 994-3957, e-mail: snayak@tqs.com

Abstract

Reliable 0.15μm gallium nitride (GaN) MMIC technology on 100μm thick and 100mm diameter SiC substrates was developed at TriQuint Texas for high volume Ku, Ka and Q-band applications. This process technology enables microwave circuit designers to pursue the market opportunities currently served by GaAs-based pHEMT MMIC technology. GaN MMIC could be an economically viable technology for commercial applications due to it's high RF output power per chip area. At 30GHz, we have demonstrated 0.15um GaN FETs simultaneously achieving an output power density of 3W/mm, power gain > 8dB, and PAE higher than 50%. This technology is very reliable with a median DC lifetime of greater than 1E7 hours at T_{ch} = 200°C with an activation energy (E_a) of 2.2eV (90% confidence interval). This robust high performance GaN technology is well suited to challenge the incumbent 0.15um power pHEMT technology.

The transistor fabrication process is summarized as follows. Source drain ohmic contacts are formed by Ti/Al alloy to GaN HEMT epitaxial layers. Active areas of the device are formed by RIE etching of a mesa in AlGaN/GaN epitaxial structures. Gates in this technology are fabricated using e-beam lithography and plasma etching of silicon nitride. A source connected second field plate is fabricated over the gate channel to suppress high electric field degradation of devices. TriQuint's 3 level metal interconnect (3MI) process is used to fabricate passives and interconnects. Wafers are thinned down to 100μm. Backside Via hole formation is done by ICP etching of SiC via holes and a backside ground plane is formed by electroplated Au.

Typical DC characteristics of the transistors are, I_{max} = 1.15A/mm, $g_{m, max}$ = 425mS/mm and pinch off voltage = -3.2V at V_{ds} = 10V. Gate-to-drain device breakdown voltages measured at I_{gd} = 1mA/mm and V_{gs} = - 6.0V exceeds 75V. Typical power density of a pre-matched 8x50 μm transistor biased at V_d = 20V, I_{dq} = 100mA/mm in a PAE tuned condition is 3W/mm at 30 GHz. Power gain and PAE of the transistors at the PAE tuned conditions are greater than 8dB and 50% respectively. Two standard products are a 4W 30GHz HPA and an 8W 30GHz HPA MMIC. Figure 1 and Figure 2 show typical performance of the 4W and 8W high power amplifiers (HPA) in fixture, respectively. As shown in Fig. 2, this GaN on SiC HPA produces greater than 8W continuous wave (CW) output power and > 25% power-added-efficiency (PAE) across the frequency band of 27 to 32GHz. To our knowledge, these results are best reported power performance for Ka-band MMICs. Several standard products including wideband PA and LNA are in development. This presentation will focus on the development methodology, product data from a number of designs (Ku, Ka, and wide-band) and the procedure to monitor the technology performance.

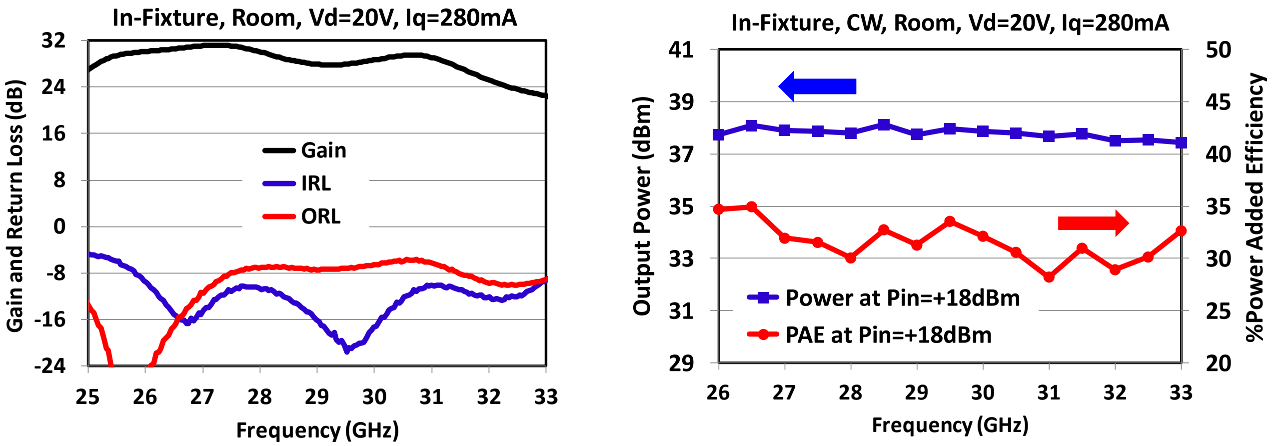

Figure 1: Measured S-parameter and (continuous wave) output power and PAE of ~ 30% responses of fixtured 4W HPA.

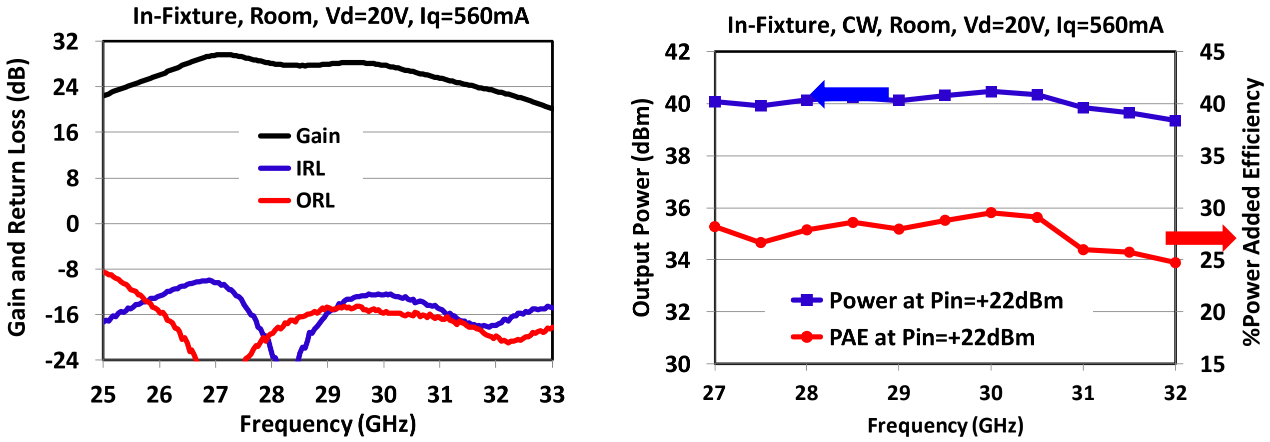

Figure 2: Measured S-parameter and (continuous wave) output power of > 8W (40dBm = 10W) and PAE responses of fixture 8 W HPA.