SiC / GaN via process – in search for perfection

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Abstract

SiC/GaN via etch and via loop process integration were studied. A new etch process region has been developed that produces nearly perfectly smooth via side wall. Side effect of other processes in the via loop was minimized for improved via quality.

INTRODUCTION

The interest in GaN devices in semiconductor industry for high power application keeps increasing in recent years. For example, nearly fifty percent of papers presented in CS MANTCH conference in 2014 were GaN related. GaN has high breakdown voltage, high electron mobility and saturation velocity [1], making it a very attractive material for many applications including high-power, high speed, and high-temperature microwave applications [2-3].

Although excellent in electric performance, GaN device has its own challenges in some of its device fabrication processes. For example, presently the majority of GaN devices were developed using SiC as the substrate for GaN growth. The etch rate of SiC is still limited to about 1um/min, much lower than that of GaAs (GaAs etch rate can easily be made to ~ 6um/min or higher). Slow etch rate of SiC means that robust masking is needed for backside SiC and GaN via etch process. Depending on the etch process conditions, as much as ~8-10 um metal hard mask was used in some cases [4,5]. SiC/GaN via formation utilizing a metallic hard mask made the overall via formation process much more difficult than that for GaAs via.

For example, using some metal mask, there is a tendency to form a layer of metal containing by-product inside via on via side wall after via etch. One may use wet chemical to etch away the metal containing by-product after SiC etch and before GaN etch. However, doing so would very likely also etch away the metal mask. As evidenced in a previous report [6], removing metal mask before GaN etch can potentially introduce an undesired notching effect at the bottom of via. In addition, it is not uncommon to observe that via side wall is rough. A rough via side wall can potentially trap residue inside and cause difficulties in subsequent conformal via side wall metallization.

It would therefore be preferable that, first of all, the by-product formation in via side wall be minimized; and secondly, the by-product, once formed, be removed without using a wet etching process that would also attach the mask or metal under the via. To be able to remove the by-product without such a wet etching process, it is desirable that via side wall be made smooth, especially if the lateral dimension of the via is much smaller than its depth. Typically, larger via diameter can have higher etch rate, making it easier to produce. A smooth via side wall will likely make the by-product removal more effective without utilizing a wet etch process.

In this paper, we report the results of SiC/GaN via formation with very smooth via side wall for small diameter vias in 100um thick SiC substrates.

EXPERIMENT

Most of the tests reported in this paper were conducted on 100 mm GaN wafers with GaN grown on SiC substrates. After completing front side of device fabrication processes, the SiC substrate is then ground and polished to its final thickness (typically 50um to 100um). A via pattern of various sizes was formed on the SiC surface. A via etch mask was deposited onto SiC surface. Optimized process was extensively tested on production wafers to demonstrate the repeatability of the result.

For SiC/GaN via etch, inductively coupled plasma (ICP) etch tool with optimized ICP source was used. Details of some of the SiC etch processes have been described elsewhere previously [7-8]. But a variety of new etching conditions were tested in this study, under different reactant composition (different gas species and different gas flow rate), process pressure, RF power, and wafer-to-plasma source spacing.

Optical microscope was used for general via inspection. For more detailed analysis, via was analyzed using SEM, FIB, and EDX to study via shape, via side wall surface topography, and the chemical composition at the via side wall surface.

RESULT

It is worth of to first note that, sample preparation appears to have substantial effect on the quality of etched via. This is shown in FIG1, where the via for both FIG1 (a) and FIG 1(b) were etched under very similar etch conditions. The via side wall is substantially different between the two samples. This

is believed to be primarily due to variation of via mask. Via hard mask for FIG 1(a) has better defined circular shape, while that for FIG 1(b) the via perimeter on the top surface is rougher than that of FIG 1(a). Bearing this potential variation of mask in mind, subsequent etching process optimization was taken place using samples cut from the same wafer.

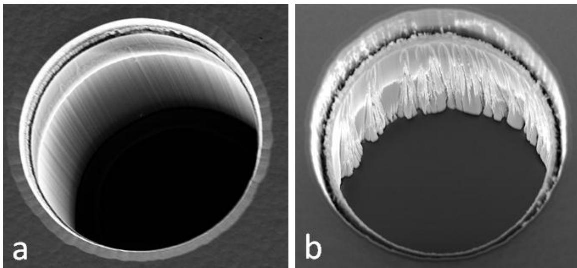

FIG.1 via from two different wafers etched under similar conditions, showing the effect of sample on via side wall.

FIG. 2 compares via etched under two different etch conditions for samples cut from the same wafer. (These samples were not cleaned after etch.) On the right, FIG 2(b), under an un-optimized etch condition, via side wall was very rough. While on the left, FIG 2(a), as etch condition moved to a different process region, via side wall became much smoother. This demonstrates the effect of etching condition on the quality of via side wall. Improved etching result of small samples (FIG. 2(a)) was repeated in full wafers, FIG. 3

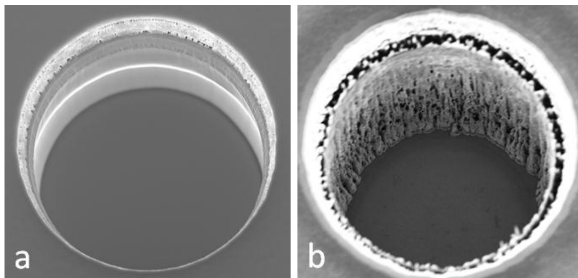

FIG 2 Via from two samples cut from the same wafer but etched under two different conditions, showing the effect of etch condition on via side wall. (a) sample etched under an optimized condition; (b) sample etched under an un-optimized condition. None of the samples was cleaned to remove side wall residue after etch.

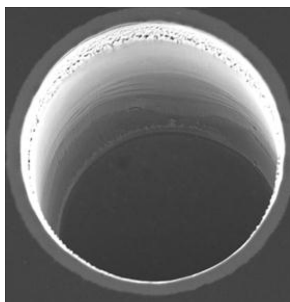

FIG 3 Typical via in full wafers etched under an optimized condition. Wafer completed all process steps except backside metallization.

To examine the via of optimized process in details, some via was cut and their cross-section view is shown in Fig. 4 (the overall shape of via) and Fig. 5 (a section of via near its bottom where it makes contact with front side metal, circled in Fig. 4).

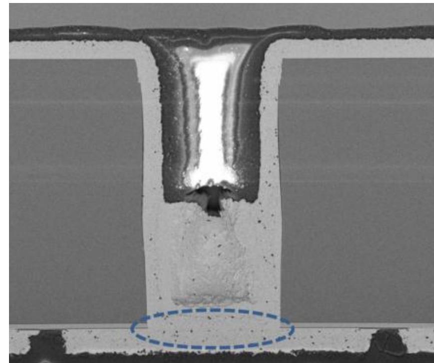

Fig 4 Cross section of a completed via. (some of the filling material inside the via is artifact of lapping process before imaging.)

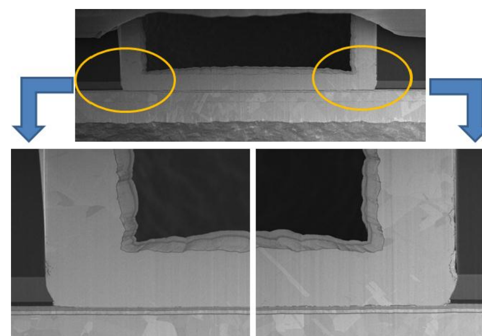

FIG 5 FIB-cross section of a via near its contact with front side metal (circled in Fig.4). Top: a section of a via near metal contact; bottom: magnified view near the corners of the via.

Fig. 2(a) and Figs. 3-5 show that the side wall of via etched using optimized process is smooth, and the overall via profile and contact with front side metal is excellent. Additional analysis using EDX indicates that there is no appreciable amount of foreign materials left on via side wall after a gentle clean. This can be seen in Fig. 6, where the EDX signal only showed the presence of Si and C, the primary composition of SiC.

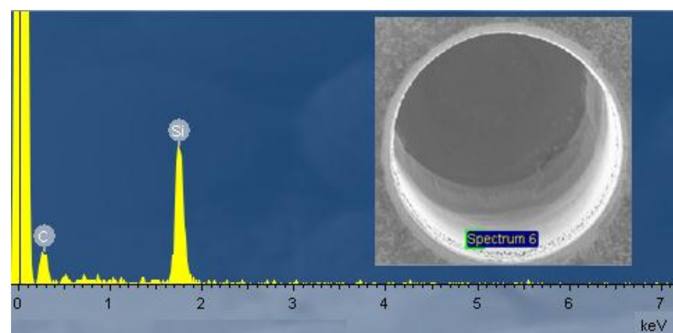

Fig. 6 EDX spectrum of via side wall.

DISCUSSION

Results presented previously shows that, although in most cases SiC / GaN via can be free of pillar [6], via side wall can be rough under some un-optimized etching condition. As etching process is moved to a more favorable region, via side wall can be substantially smoothened in addition to free of pillars formation at the bottom of via. Via side wall can also be free of foreign materials as confirmed by EDX spectrum. However, in practice, it is not convenient to monitor the etch result using SEM for all wafers and for all via in a production environment. We note that in most cases, an optical inspection can easily reveal the quality of via side wall without much ambiguity. A via with rough side wall often does not have well defined shape as the original via pattern, while via with smooth side wall maintains the shape of its original pattern, see Fig 7 as an example for circular via. The circular pattern was seriously distorted in Fig. 7(a) due to side wall roughness. For via with smooth side wall, the via at the bottom maintains a perfectly circular shape, Fig. 7(b).

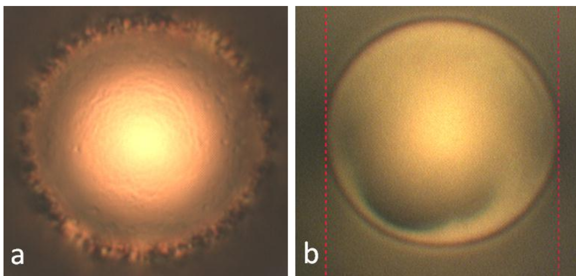

FIG 6 Optical image of via at the bottom after SiC / GaN etch. (a) Via with rough side wall, and (b) via with smooth side wall.

The optimized etch process can extends well to high aspect ratio vias, where aspect ratio is the ratio between via depth and via diameter for circular via, or between via depth and via width for square or rectangular vias. Via side wall is smooth and bottom of via is substantially free of pillar formation for square via with aspect ratio ~3, see Fig.7.

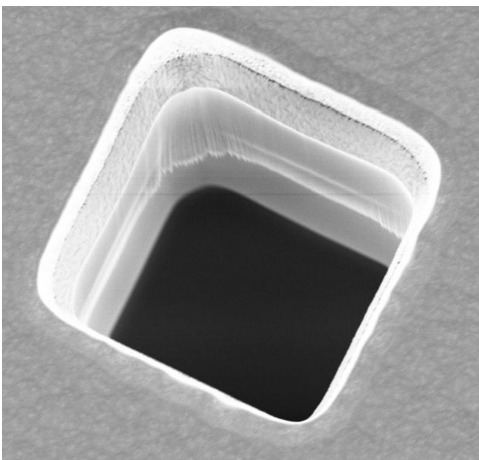

Fig. 7 Cross-section of a square via with aspect ratio 3.

CONCLUSION

Various factors such as via hard mask can have big effect on via side smoothness. A new etch process has been developed that produces nearly perfectly smooth via side wall and is less sensitive to other variation such as via etch mask. This etch process has been demonstrated to be extendable to small via in SiC substrate with aspect ratio of 3. It is also shown that very simple optical inspection can be used as a first gauge of via side wall quality without utilizing SEM inspection. This substantially simplifies the inline inspection process in production environment.

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ACRONYMS

ICP: Inductively Coupled Plasma