pHEMT Device Characterization for Current Transient Time Constant and Link to Error Vector Magnitude

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Introduction

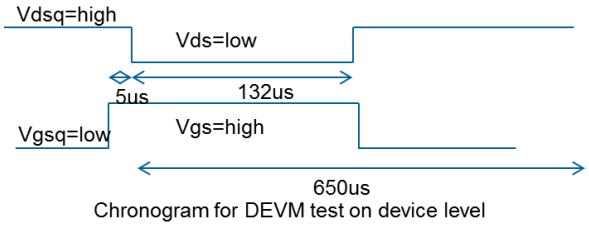
The most challenging design and materials issue for future wireless LAN circuits remains dynamic error vector magnitude, or DEVM. While circuit designers have some ability to overcome materials-based current transients, eventually manipulating the fundamental materials is necessary to meet increasingly demanding customer specifications for DEVM. In some of our early WLAN designs the challenges and rewards of DEVM control became obvious, manifesting in yield fluctuations. Extensive testing of different epi and device processes and designs made it clear that circuit performance was linked to both the epi and fab. However, the mechanism for epi and fab impacts on circuit performance was not clear. In this work, we will describe a single-FET characterization technique that predicts circuit-level challenges for DEVM control.

Purpose

This paper describes a measurement flow for single device characterization under DEVM conditions. The technique used pulsed IV in a conceptually simple measurement that was fully descriptive of the problem, and the difference between devices. The measurement consists of three separate transient measurements. Each measurement is necessary to understand the contributions from each region of the device to total transient time constant. Understanding the source of the transient and trapping behavior and the correlation to DEVM performance helps design teams to make the connection to DEVM data on circuit level. The technique is also beneficial in epi design and supplier qualification. With device level characterization, it is possible to synthesize device and epi understanding to improve circuit performance and yield.

DEVM measurement on device level

DEVM was measured at final test and is correlated to a deviation of drain current from an expected value during the data burst. Delays in current response can be caused by charge-trapping process. Delays can further be added by circuit design when the design is optimized for a specific fab lot or epi supplier, but drift in the epi growth or fab process occurs. Thus, it was necessary to separate the influence of design and device performance on DEVM by defining an approach for device level characterization. The chronogram for DEVM test on device level is shown in Figure 1. The measurement is performed using Pulsed IV system (IVCAD) where the transient response is obtained in real time.



Chronogram for DEVM test on device level

Figure 1: Chronogram for device level DEVM test

Transient response was measured on the device level under DEVM conditions for two different epi designs within a single fab process lot. The resulting Ids change over time shows clear differences in the drain current change versus time for materials A and B (Figure 2). This result matched what was observed on the circuit level, but measured delays in drain current response were still a combination of thermal, drain and gate lag time constants. The goal was to apply test conditions to separate factors contributing to the overall time constant. This would allow identification of the dominant cause of variation that contributes to performance variation in the finished circuit. The three-step test flow is shown in Figure 3.

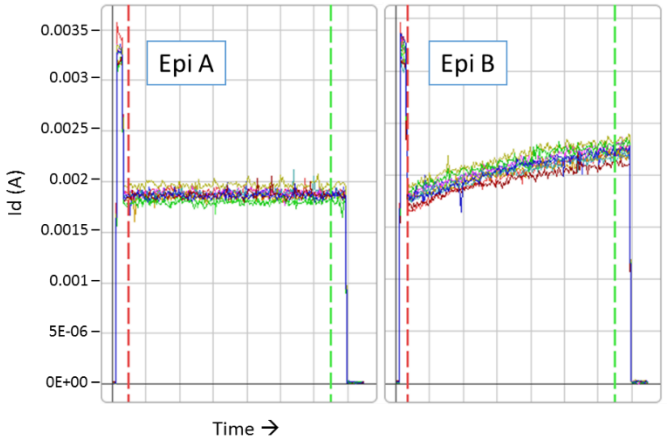


Figure 2: Transient response of device from two epi wafers under DEVM conditions

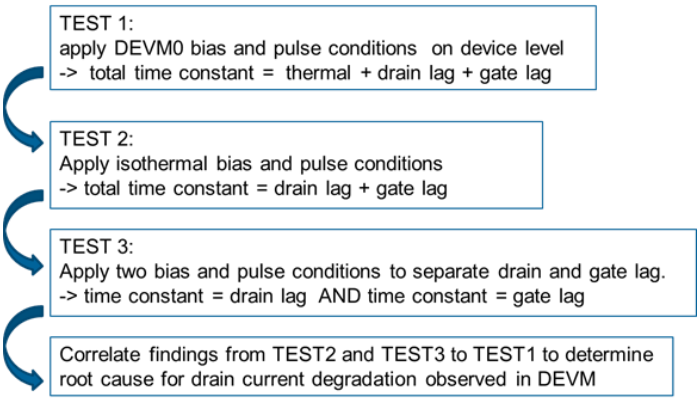


Figure 3: Test flow for transient characterization

In the test flow, each individual test isolates a region of the device to identify performance-limiting aspects of the fab and epi processes. For example, test 2 measures transient response under isothermal conditions. This approach isolates trap behavior from thermal effects. The results of this test are shown in Figure 4 for two different power levels (Pdiss=0.033mW/um^2, 3.3mW/um^2) for two different epi types. The main difference between epi types is in the emission time constant, or de-trapping.

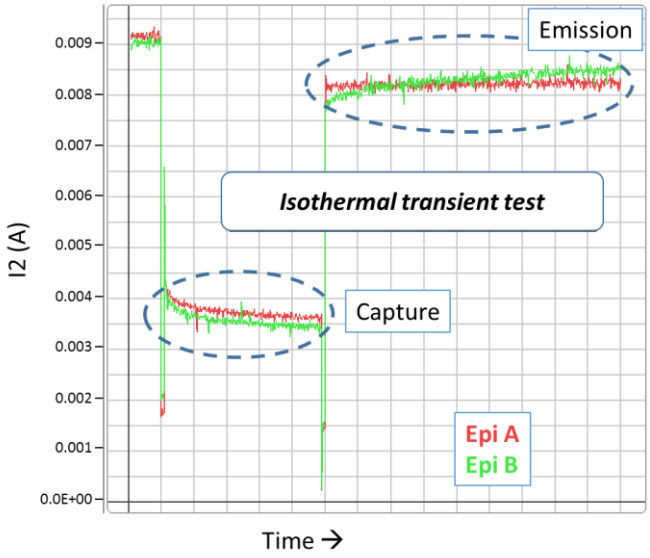


Figure 4: Transient response for test 2, isothermal transient test on two epi types

Both epi types showed that under drain lag conditions, when drain voltage was changed from high to low value, main difference is in de-trapping time constant and that device with good DEVM response is not actually "trap-free" (capture time constant was in order of 10's usec) but the release of traps took longer for epi A and thus did not impact DEVM results as the de-trapping time constants was much longer.

The observed differences demonstrate how a simplified test can show specific areas of the device for focused improvement. Previously, SIMS, cross-sections and PCM data were the main clues for yield improvement and supplier matching. With this improved test flow, we will demonstrate that tests 1, 2 and 3 are all required for a complete understanding of the device impacts on circuit-level performance.

Conclusion

Transient data revealed not only the magnitude but also the mechanism for differences in drain current response under DEVM conditions. The measurement flow presented for trapping characterization can also be applied to other devices such as GaN HEMTs. Having a simple, device level method to quantify time constants for different device processes is useful not only for design but also in process and epi supplier qualification.