Field Plate Models Applied to Manufacturability and RF Frequency Analysis

Robert Coffie
RLC Solutions, LLC, 6520 Tearose Dr., Plano, TX 75074
Phone: (972) 767-9388 e-mail: rcoffie@rlcsolutions.com

Introduction

Field plates are now commonly used for electric field engineering in both high frequency and power transistors. With proper field plate design, significant performance improvements can be obtained [1]. Despite the wide spread adoption of field plates, only recently has a simplified field plate model that captures the majority of the physics been introduced [2,3].

It is the purpose of this work is to demonstrate how the simplified field plate model in [2,3] can be used by the process engineer for an electric field sensitivity analysis on sidewall angle between field plate and gate and on field plate to channel spacing (a_1). Building on the two transistor model for a transistor with a field plate also introduced in [2], it will be shown how the device designer can use circuit simulation tools or standard circuit analysis to analyze high frequency operation of transistors with field plates.

Field Plate Model

The field plate model introduced in [2,3] will be developed from a charge imaging standpoint during the presentation. The model is only valid for long field plate designs. A natural definition of long comes from the model through the aspect ratio of field plate length (including slant portion) to a_1 be ≥ 6. An aspect ratio of ≥ 6 follows the well-known aspect ratio design rule used for gate length designs now being seen to also apply to field plates. It also supports the view of analyzing the field plate and gate as a combination of two transistors in series with one transistor representing the gate and the second transistor representing the field plate as shown in Fig 1.

The model also shows that independent of transition angle, the pinch-off voltage of the field plate can be viewed as the maximum channel potential between gate electrode and channel. Therefore, the difference between the potential applied to the field plate and the field plate pinch-off voltage can be viewed as the drain voltage applied to the transistor representing the gate electrode (Q1) in the two transistor model as shown in Fig 1.

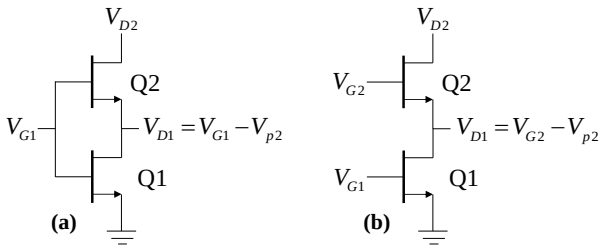

Fig. 1. Two transistor model for an FET with a field plate. (a) Equivalent circuit of gate connected field plate. V_{DG1} is always $-V_{p2}$. (b) Equivalent circuit of field plate not connected to gate. $V_{DG1} = V_{G2}-V_{G1}-V_{p2}$.

Building upon these results, it will be shown how electric field sensitivity analysis on process controlled parameters can be performed and how the two transistor model for FETs with field plates can be used for frequency performance analysis.

Sensitivity Analysis

In order to produce a stable repeatable process, understanding design sensitivities to process controlled parameters is key. The field plate model introduced in [2,3] allows investigating electric field sensitivity on both transition angle between gate and field plate as well as on a_1. Brief analysis for the electric field dependence on a_1 will be given, with the presentation and full paper containing the complete electric field sensitivity analysis for sidewall angle and a_1.

To understand the sensitivity of peak electric field in the channel on field plate distance to channel (a_1), the model was used to simulate different field plate to channel distances for the relatively insensitive transition angle of $90°$. Figure 2 shows the peak electric field in the channel as a function of a_1/a_0 (field plate to channel distance normalized to gate to channel distance). An almost linear

relationship exist. The sensitivity of the peak electric field to a_1/a_0 is:

$$\frac{d\mathcal{E}_{peak}}{d\left(a_1/a_0\right)} = 0.16 - 0.0045\left(a_1/a_0\right) \qquad (1)$$

Controlling the field plate to channel distance by $\pm a_1/2$ results in about a $\pm 5\,\%$ change in peak electric field for $a_1/a_0 = 4$.

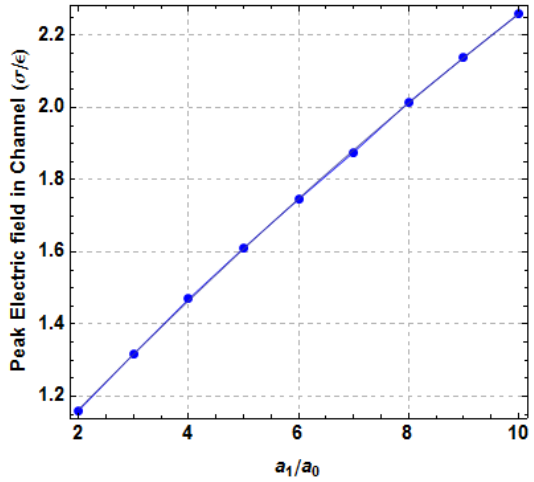

Fig. 2. Peak electric field in the channel as a function of field plate to channel distance.

Frequency Analysis

In [2], a two transistor model for FETs with a field plate was used for DC analysis. The two transistor model will now be used for RF analysis of a FET with a field plate. Experimentally, significant improvements in gain have been obtained with source connected field plates compared to gate connected field plates [1]. Using the two transistor model, the short circuit current gain (h_{21}) of a gate connected field plate, a source connected field plate, and a transistor without a field plate are given as:

$$h_{21,sc} = \frac{f_{\tau,1}}{jf}\left(1+\frac{jf}{f_{\tau,2}}\right)^{-1}$$

$$h_{21,gc} = \frac{f_{\tau,1}f_{\tau,2}}{jf\left(f_{\tau,1}+f_{\tau,2}\right)}\left(1+\frac{jf}{f_{\tau,1}+f_{\tau,2}}\right)^{-1} \qquad (2)$$

$$h_{21,1} = \frac{f_{\tau,1}}{jf}$$

where $f_{\tau,1}$ and $f_{\tau,2}$ are the unity short circuit current gain frequencies associated with the transistor representing the gate and field plate, respectively, and $h_{21,1}$, $h_{21,gc}$, and $h_{21,sc}$ are the short circuit current gains of a FET without field plates, a FET with a gate connected field plate, and a FET with a source connected field plate, respectively. A plot of $|h_{21}|$ vs. $f/f_{\tau,1}$ with a typical value of $f_{\tau,1}/f_{\tau,2} = 2$ are shown in Fig. 3. A significant improvement in h_{21} when using a source connected field plate compared to a gate connected field plate is observed. In fact when viewing field plated FETs as two transistors, gate connected field plates are configured opposite the traditional approach for high frequency device pairs such as Darlington pairs or f_τ-doublers where the inputs are connected in series and outputs are connected in parallel. Using this same approach, restrictions on $f_{\tau,2}$ or power gain parameter such as the maximum frequency of oscillation $f_{\max}$ can be translated into field plate constraints for high frequency device design with field plates. Other examples will be given in the full paper and presentation.

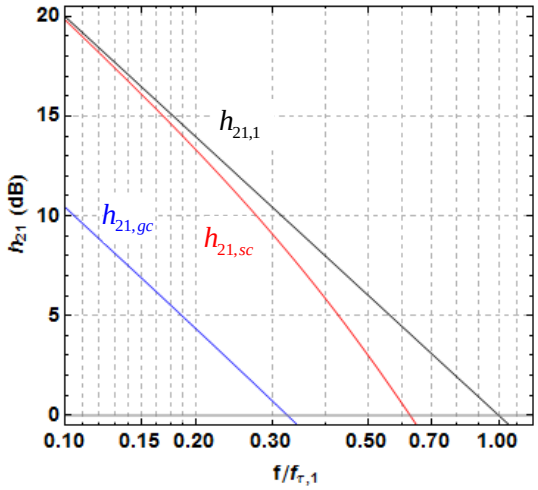

Fig. 3. H21 comparison for a gate connected field plate FET, source connected field plate FET and FET with no field plates.

References

1. Y.-F. Wu, et al., "High-gain Microwave GaN HEMTs with Source-terminated Field-plates," Proceedings of IEDM, pp. 1078 – 1079, Dec. 2004.
2. R. Coffie, "Analytical Field Plate Model for Field Effect Transistors," IEEE Trans. Electron Dev., vol. 61, no. 3, pp. 878 – 883, March 2014.
3. R. Coffie, "Slant Field Plate Model for Field Effect Transistors," IEEE Trans. Electron Dev., vol. 61, no. 8, pp. 2867 – 2872, August 2014.