

# A CMOS-compatible Fabrication Process for Scaled Self-Aligned InGaAs MOSFETs

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## Abstract

We have developed a scalable gate-last dry recess process to fabricate planar InGaAs Quantum-well (QW) MOSFETs. The fabrication sequence yields precise control of all critical transistor dimensions, in particular, the length and thickness of the channel and access regions. The process relies on a combination of anisotropic and isotropic F-based dry etching of Mo ohmic contacts that are formed early in the process. Anisotropic Cl-based dry etching is used to recess the In-based III-V cap material. This is followed by a digital etch technique that achieves a depth control down to sub-1 nm. We demonstrate  $L_g=20$  nm MOSFETs with 15 nm contact-gate separation and good electrical characteristics.

## Introduction

InGaAs is a promising candidate for channel material for future CMOS due to its superior electron transport properties [1]. Several self-aligned device architectures have been demonstrated, such as the Recessed Gate [2-5], Implanted Source and Drain (SD) [6-7] and Regrown SD [8-9]. Among these, the recessed-gate technology is attractive due to its scalability and simplicity. It has also yielded outstanding performance results [4-5]. This paper describes in detail a self-aligned recessed-gate process that has yielded record transconductance scaled InGaAs MOSFETs. Our fabrication process takes CMOS compatibility into consideration with extensive use of dry etching being made to insure tight pitch, low parasitics and high manufacturability.

## Device Fabrication Overview

At the heart of the fabrication process of our recessed-gate InGaAs QW-MOSFETs is the gate recess sequence of Fig. 1. The starting wafer is grown by MBE by *IntelliEpi*. The process starts with a W/Mo ohmic contact stack sputtered on the as-grown epitaxial structure. After E-beam gate patterning, a SiO<sub>2</sub> mask and the W/Mo contact stack are etched by F-based *anisotropic* RIE (Fig. 1a). W serves as barrier against Mo oxidation during SiO<sub>2</sub> CVD and mitigates a deep undercut into the Mo that is produced otherwise [3]. After resist removal, a second F-based *isotropic* RIE is used to laterally undercut the ohmic metal in a controlled manner (Fig. 1b). This is achieved by adding O<sub>2</sub> during RIE [10]. The RIE time controls the lateral recess depth which eventually sets the final length of the device access regions.

F-based RIE stops on the III-V surface. To recess the III-V cap, anisotropic Cl-based RIE is used. This etching is not selective and is controlled by etch time. By calibrating the etch rate, we can stop the cap recess a few nanometers above the channel (Fig. 1c). Annealing at 340°C for 15 min is applied to repair the RIE damage [2]. Beyond this, digital etch (DE) is used to precisely bring the recess to the desired depth [5,11]. This also sets the thickness of the access region (Fig. 1d). Our digital etch approach consists of native III-V oxide formation through exposure to low power oxygen

plasma, followed by oxide removal in diluted H<sub>2</sub>SO<sub>4</sub>. This process is self-limiting and has a resolution of 0.9 nm/cyc [11]. We have demonstrated a technique that takes advantage of the high selectivity of certain chemical etchants for InGaAs over InP (used as etch stop layer) to precisely control the final channel thickness with a precision of 1 nm [11]. This is confirmed by TEM [5]. After the last DE cycle, a fresh semiconductor surface is exposed and this is immediately followed by ALD of 2.5 nm HfO<sub>2</sub> as gate dielectric and Mo gate metal deposition and definition. The device is completed by via and pad formation. The entire front-end fabrication closely follows CMOS compatibility requirements and is wet-etch free, lift-off free and Au-free.

## Optimization of III-V Dry Etch

The III-V dry etch is carried out in a SAMCO RIE-200iP ICP system. The baseline conditions are: gas flow Cl<sub>2</sub>:N<sub>2</sub>=10:3 sccm, pressure =0.2 Pa, ICP power=20 W, substrate bias voltage=130 V, etch time=100 s, and chuck temperature 120°C. Under these conditions, 20 nm of the composite InGaAs/InAlAs/InP cap structure are removed. A larger bias voltage results in higher etch rate (Fig. 2) but at the expense of increased surface roughness (Fig. 3) and considerably worse trenching caused by ion deflection (Fig. 4).

Besides bias voltage, increasing the N<sub>2</sub>:Cl<sub>2</sub> gas ratio and the pressure both roughen the surface. A BCl<sub>3</sub>-based etch recipe similar to [12] was also investigated and discarded due to surface roughening. Unlike the BCl<sub>3</sub>-based recipe, our Cl<sub>2</sub>/N<sub>2</sub>-based approach shows little dependence on the substrate temperature during etch.

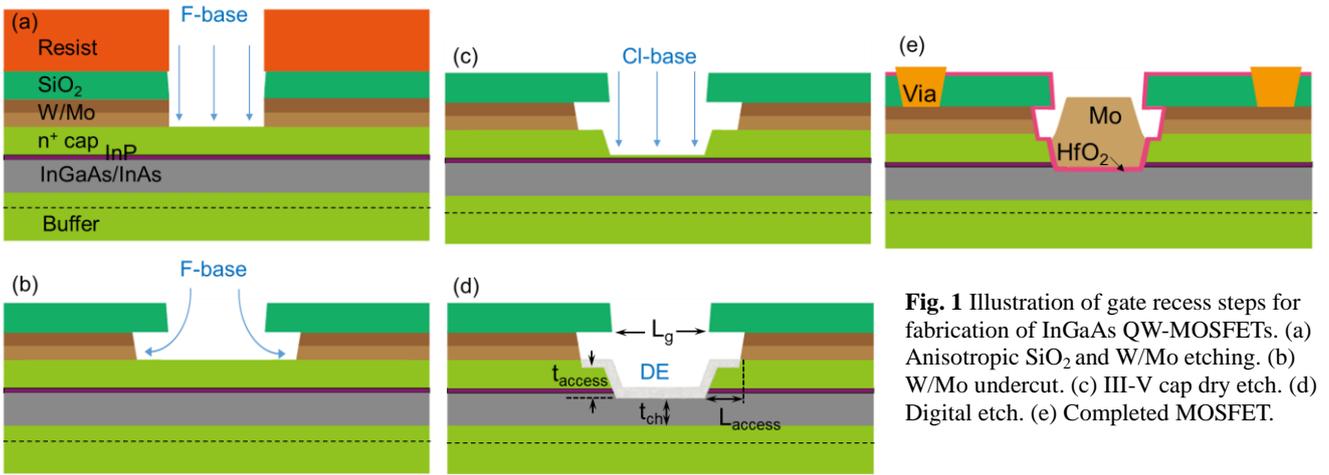
## Device Characteristics

Fig. 5 shows TEM cross sectional images of finished InGaAs MOSFETs recessed at two bias conditions during III-V cap etching (baseline [5] and slightly higher bias [4]). In both cases, nm level control of the channel thickness is demonstrated with a final thickness of 4 nm and 8 nm, respectively. Under optimized baseline conditions, a flat channel is obtained (Fig. 5a). At the higher bias, there is noticeable trenching with the channel ends being about 1 nm thinner than the center (Fig. 5b).

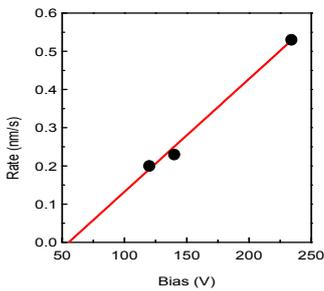
Excellent output characteristics of a fabricated  $L_g=20$  nm MOSFET with about 15 nm separation between the edge of the ohmic contacts and the edge of the gate (Fig. 6) demonstrate the potential of our technology for highly scaled tight pitch InGaAs MOSFET fabrication (Fig. 7).  $L_g=80$  nm devices with a record  $g_{m,max}$  of 3.1 mS/ $\mu$ m at  $V_{ds}=0.5$  V have also been demonstrated [5].

## Conclusions

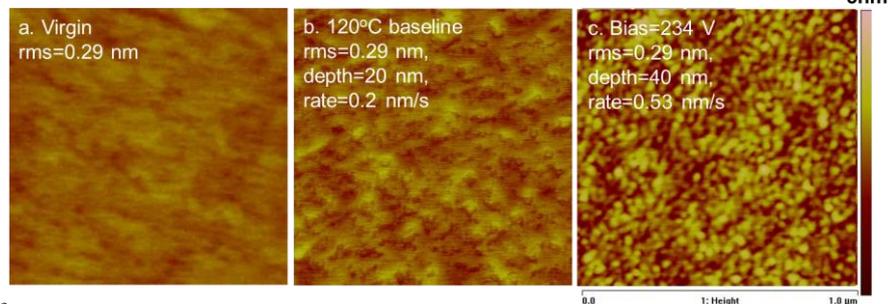
This work describes a novel dry-etched recessed-gate process to fabricate extremely scaled self-aligned InGaAs MOSFETs. We achieve a smooth etched intrinsic surface with minimum trenching. Recess depth control within 1 nm accuracy can be achieved. Fabricated devices demonstrate excellent electrical characteristics.



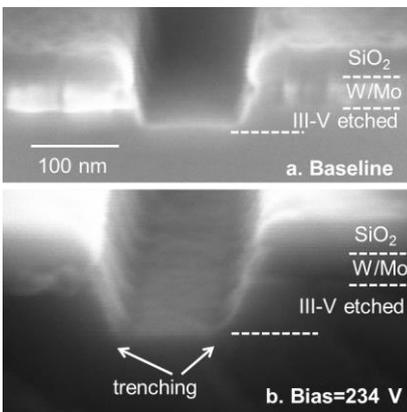
**Fig. 1** Illustration of gate recess steps for fabrication of InGaAs QW-MOSFETs. (a) Anisotropic SiO<sub>2</sub> and W/Mo etching. (b) W/Mo undercut. (c) III-V cap dry etch. (d) Digital etch. (e) Completed MOSFET.



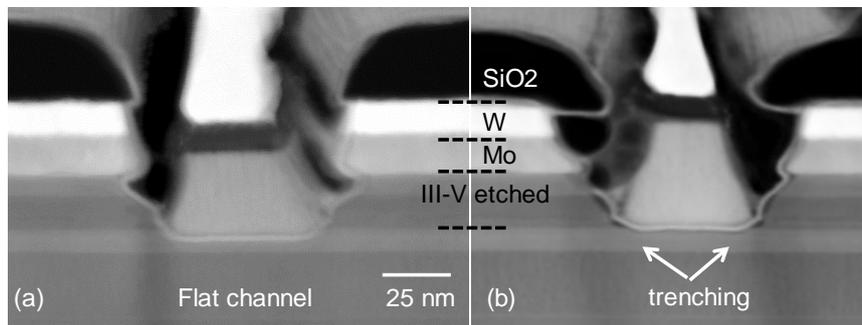
**Fig. 2** III-V cap etch rate as a function of substrate bias voltage. Threshold bias voltage for etching is about 60 V.



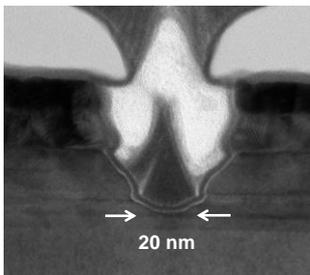
**Fig. 3** AFM surface scan for 1 μm<sup>2</sup> area on (a) virgin wafer, (b) dry-etched sample at baseline conditions, (c) dry-etched sample at higher bias of 234 V.



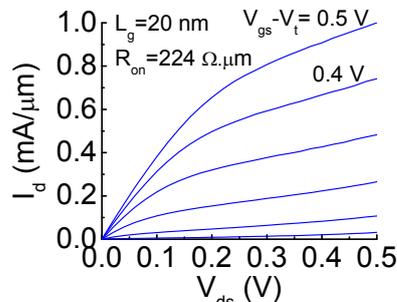
**Fig. 4** Cross section SEM images for dry etched sample using (a) baseline III-V etch conditions and (b) high bias condition. The recess opening is 100 nm.



**Fig. 5** TEM cross sectional images of finished InGaAs MOSFETs. (a) Device with 4 nm final channel thickness. The baseline dry etch recipe results in a completely flat channel, free of trenching. (b) Device with 8 nm final channel thickness. At a slightly higher substrate bias, trenching at both ends of the channel results.



**Fig. 6** TEM cross sectional image of the InGaAs MOSFET with L<sub>g</sub>=20 nm and 15 nm contact-gate separation.



**Fig. 7** Output characteristics of InGaAs MOSFET with L<sub>g</sub>=20 nm.

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