

Comparison of thermal properties of packaged AlGaIn/GaN HFETs on Si and *n*-SiC substrates

R. Zhytnytska¹, J. Böcker², H. Just², E. Bahat-Treidel¹, O. Hilt¹, S. Dieckerhoff², J. Würfl¹ and G. Tränkle¹

¹Leibniz Institut für Höchstfrequenztechnik, Ferdinand-Braun-Institut, Gustav-Kirchhoff-Str. 4, 12489 Berlin, Germany, e-mail: zhytnytska@fbh-berlin.de

² Technische Universität Berlin, Power Electronics Research Group

Purpose of the work

High voltage power switching AlGaIn/GaN HFETs are gaining considerable interest for future highly efficient power electronic applications. Due to its lower cost and production line compatibility, GaN-on-Silicon approaches are most attractive for industrial implementation. On the other hand, the Si substrate has a three times lower thermal conductivity as compared to the SiC substrate which is well established in RF technology. It is important to compare systematically power switching devices fabricated on Si substrates versus similar devices on SiC substrates in order to evaluate potential trade-offs.

Here, we present a method of thermal characterization of AlGaIn/GaN HFETs based on pulsed electrical measurements (dynamic IV analyses (DIVA)). First we compare small test transistors (two fingers, 0.25 mm gate width), on Si and SiC substrates and demonstrate the increased self-heating for the GaN-on-Si devices. Then we demonstrate pulsed characterizations of large periphery 60 mΩ AlGaIn/GaN HFETs with 214 mm gate width up to 120 A at base-plate temperatures up to 150 °C.

Device fabrication and measurement setup

All small devices are processed on MOCVD grown GaN-on-Si wafers from a commercial vendor and GaN-on-SiC wafers from FBH epitaxy using Schottky gate technology [1]. The large periphery transistors are processed using FBH's p-GaN gate technology [2]. All devices have a gate-drain separation of 15 μm. The devices are cut out to a 3.6 × 2.8 mm² chip size for the 0.25 mm devices, whereby the transistor is placed in the middle of the chip, and 4.4 × 2.3 mm² chip size for the 60 mΩ transistors. Chips are soldered on an Au-coated CuMo heat sink using a PbSn₅Ag_{2.5} solder alloy and connected by Au wire bonding.

The characteristics of small devices are measured with by DIVA at $V_{gs} = +1$ V for $V_{ds} = 0...20$ V at base plate temperatures varying from 25 to 125 °C for pulse lengths of 0.2, 2, 20, 200 and 500 μs and statically (see fig. 1). For calibration purposes we first extract the data along the hyperbolic curve of constant dissipated power for power densities between 2 and 7 W/mm at short pulses of 0.2 μs for different base plate temperatures. At this condition the self-heating of transistor is negligible and the decrease of drain current with increasing temperature can be calculated for each power condition. This provides a thermal coefficient of drain current (α_{th}). Based on α_{th} , the average channel temperature can be calculated by analyzing the drain current decay at different pulse durations and different heat dissipation. The measurement results have been compared to thermal transient simulation (ANSYS) of idealized GaN-on-Si and GaN-on-SiC structures.

A measurement setup, comparable to DIVA, designed for current capability up to 200 A has been developed at TU Berlin for the large transistors. Devices have been pulsed with a pulse length of 5 μs from off to on-state ($V_{gs} = +5$ V) and back (see fig. 3A). The dynamic IV characteristics have been extracted at various time-windows within the pulse (at 0.6...1, 1.7...2.3 and 4.4...4.7 μs after the switching event).

Results

Fig. 2 shows the average channel temperatures (T_{ch}) extracted from measurements at different pulse durations and power dissipation levels. At a thermal dissipation of 7 W/mm and 500 μs pulses devices on GaN-on-Si wafers heat up to 180°C whereas the maximum channel temperature for devices on GaN-on-SiC wafers piles up to 55°C only. The resulting R_{th} is ~ 5 times higher for GaN-on-Si device. The simulated average T_{ch} is well in agreement with the measurements for GaN-on-SiC devices whereas the simulation for GaN-on-Si devices predicts considerably lower thermal impedance as measured in found in experiment. This means, that additional thermal barriers might be buried in the Si-GaN-AlGaIn epitaxial stack and they are most probably attributed to an additional thermal boundary resistance (TBR) effect.

During short pulse measurements large periphery transistors on SiC substrate generally show similar thermal dependencies as the smaller transistors. At a pulse length of 1 μs for example the thermal dependent current drop of $I_{ds,max}$ at different base plate temperatures of 25°C to 125°C is with 34 % the same as for the small devices. However for increasing pulse length the heating effect on large device is more pronounced. The significant lateral heat spreading in the SiC substrate causes better cooling of the small devices. According to the observed higher R_{th} , we assume that the I_{ds} drop caused by power dissipation could significantly affect the performance of AlGaIn/GaN HEMTs on Si substrate. Careful thermal management of such devices will be important in order to increase the efficiency of AlGaIn/GaN power transistors on Si substrate.

- [1] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, H.-J. Würfl and G. Tränkle, "AlGaIn/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1 kV and low $R_{ON} \times A$," *Electron Devices, IEEE Transactions on*, vol.57, no.11, pp.3050-3058, November 2010.
- [2] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel and J. Würfl, "Normally-off AlGaIn/GaN HFET with p-type GaN Gate and AlGaIn Buffer", *Proc. ISPSD 2010, Hiroshima*, pp. 347-350.

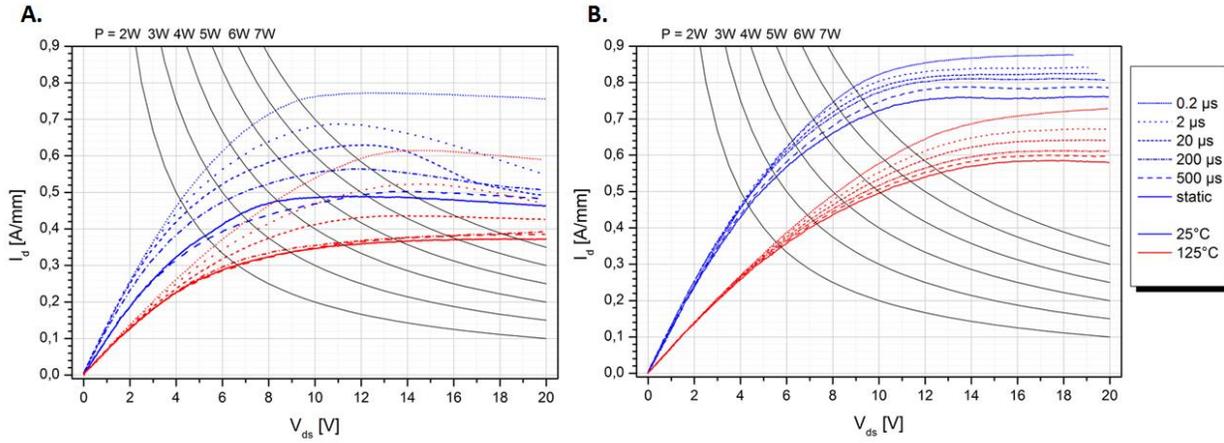


Fig.1: Pulsed and static IV characteristics of small devices measured at $V_{gs} = +1$ V for pulse lengths from 0.2 to 500 μ s at base plate temperatures from 25 to 125°C: **A.** GaN-on-Si, **B.** GaN-on-SiC wafer.

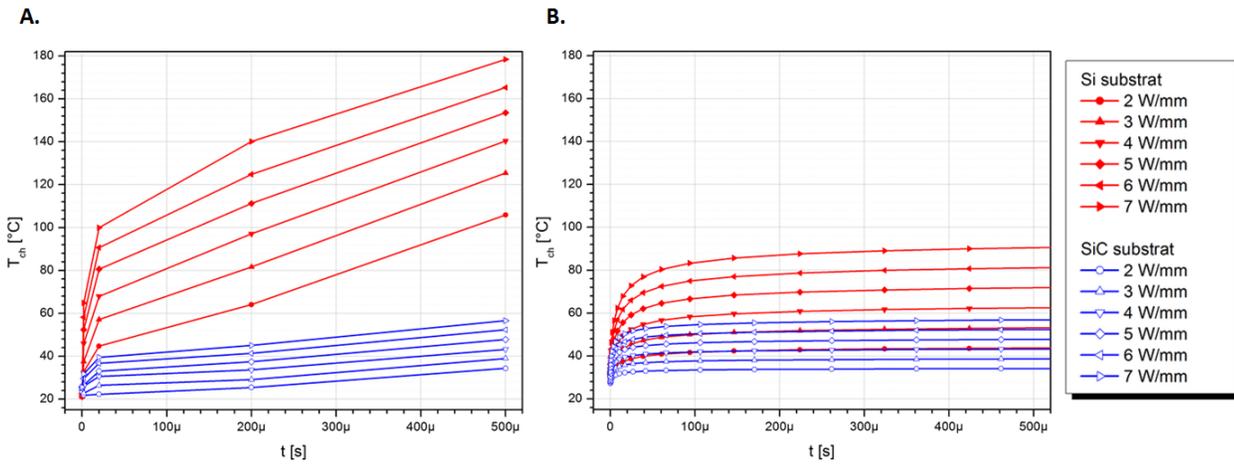


Fig.2: Comparison of average channel temperature (T_{ch}) in dependence on time after switching event for small devices on GaN-on-Si and GaN-on-SiC wafers. Parameter: Different levels of dissipated power. **A.** calculated from pulsed IV characteristics, **B.** simulated on idealized structures with ANSYS.

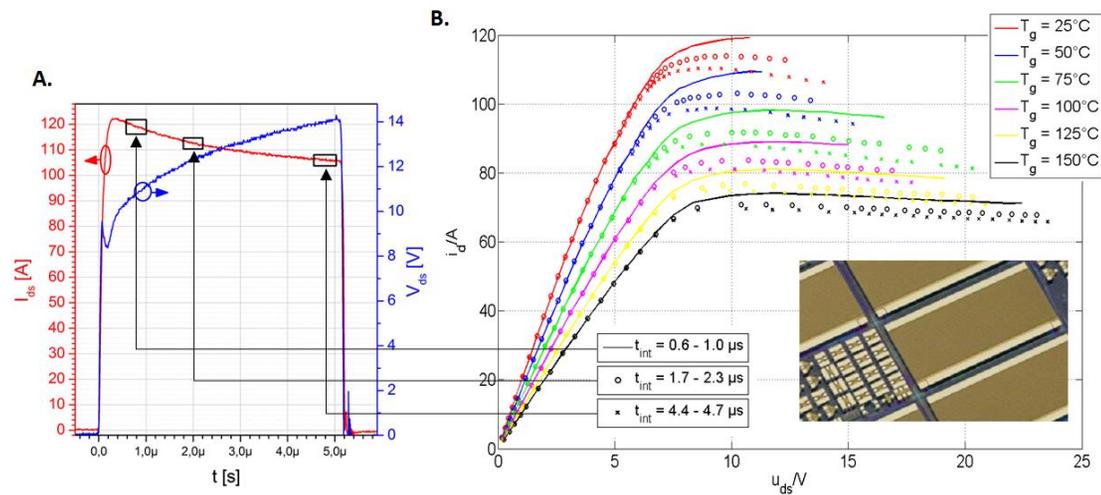


Fig. 3: **A.** Example of pulsed IV characterisation of large periphery devices fabricated on SiC substrates, pulse duration 5 μ s. The marked time windows represent the measured intervals for IV characteristic extraction according to fig. 3B. **B.** Extracted output characteristics (taken at $V_{gs} = +5$ V at different timing after pulse turn-on. Base plate temperature varies between 25 to 150°C).