Current Dispersion in Short Channel $Al_{0.32}Ga_{0.68}N$/GaN HEMTs

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Current work presents investigations of short channel AlGaN/GaN HEMTs with L_g varying from 100 nm to 200 nm. Primary goal was to find an optimum combination of gate length and epitaxial structure design for Ka-band operation. Thus, two epitaxial structures with different buffer layers were implemented in conjunction with nominally the same AlGaN barrier and GaN cap layers. Fabricated transistors were characterized using DC, small-signal, load-pull and dynamic IV measurements. The observed correlation between gate lagging and transistor's gate length has been attributed to the specific epitaxial structures. The mechanism of this phenomenon is discussed by means of a different amount of charge trapped under gates of different lengths in conjunction with the effect of gate-dependent polarization charge [1].

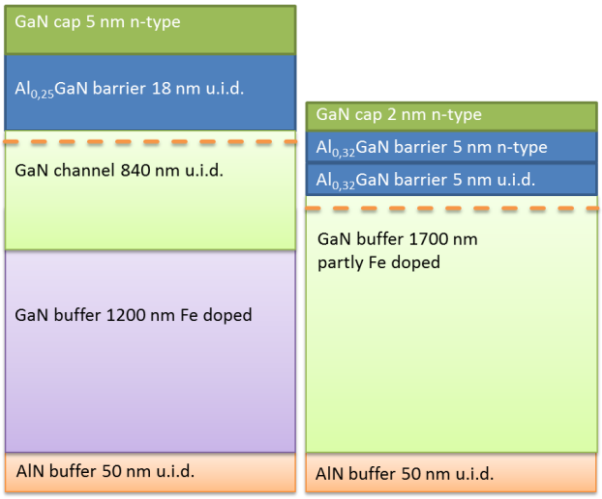

Figure 1 – Epitaxial structures used in experiment

Epitaxial structures were grown by low-pressure MOVPE on semi-insulating 4H-SiC substrates. Fig. 1 describes the detailed design of the two epitaxial versions. As known from literature [2], for optimal AlGaN/GaN HEMTs operation the L_g/t_{bar} (where t_{bar} is total thickness of barrier layers) aspect ratio should be more than 15. In case of short channel transistors (L_g < 250 nm), maintaining the ideal aspect requires rather thin barrier layers, i.e. AlGaN and GaN cap. However this compromises the 2DEG concentration and consequently decreases the output power density [3]. In order to overcome this problem, AlGaN layers with high Al content (32%) were analyzed. In detail, the barrier consists of a stack of two $Al_{0.32}Ga_{0.68}N$ layers, an undoped layer close to the channel followed by an n-type layer that provides additional channel electrons due to modulation doping. A 2 nm n-type GaN cap prevents potential surface instabilities. Barrier and cap design has been kept constant for all epitaxial designs investigated. In order to address electron confinement in the 2DEG the buffer of the first epitaxial structure (Fig.1 left) comprises a 50 nm thick u.i.d. GaN channel layer and an $Al_{0.04}Ga_{0.96}N$ back barrier layer. Due to band gap discontinuity between GaN and AlGaN layers such a design confines electrons within the channel (back-barrier approach). In addition the low carrier mobility in the AlGaN alloy furthermore increases isolating properties of the buffer. The second structure (Fig. 1 right), represents a more conventional design and contains a Fe doped GaN buffer followed by an u.i.d. GaN channel layer. The thickness of the channel layer is designed so that the Fe concentration decaying from the Fe-doped buffer drops below the SIMS detection limit at the 2DEG position. AlGaN/GaN HEMTs with various gate lengths were fabricated on these two epitaxial structures.

During the first phase of the experiment, transistors with gate lengths of 100 nm and 130 nm were fabricated on both kinds of epitaxial structures. From the shape of DC output characteristics it has been found that the epitaxial structure with GaN:Fe buffer provides much worse electron confinement as compared to the epitaxial structure with AlGaN back barrier. The latter ones work well down to gate lengths of 100 nm. The disadvantage of the AlGaN back barrier structure is a much lower 2DEG concentration, and, consequently, an almost halved drain current compared to the structure with GaN:Fe buffer. It was observed, that for the epitaxial structure with GaN:Fe buffer it is impossible to achieve reliable transistor pinch-off with 100 nm gate length. Therefore, it was decided to use 150 nm and 200 nm gates in the second phase of the experiment. Transistors with the gate lengths of 150 nm were fabricated on an additional wafer with AlGaN back barrier buffer in order to provide valid comparison based on

the 150 nm gates. In order to explore the properties of the shorter gates this particular wafer contained transistors with 100 nm gates as well.

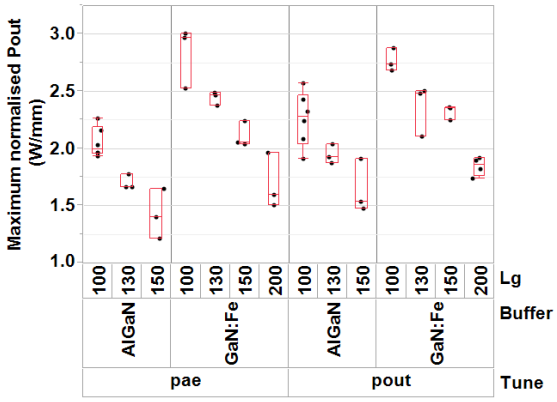

Figure 2 – Results of load-pull measurements of 8×100 µm transistors at 10 GHz

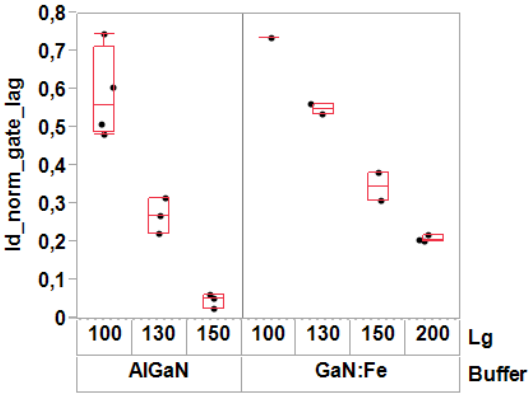

Figure 3 - Normalized drain current drop caused by gate lag

Fig. 2 shows the results of load-pull measurements at 10 GHz obtained for 8×100 µm transistor design. Measurements were performed at two bias points at V_d = 28 V and I_d = 10 % and 30 % of I_{d_max} with the load impedance optimized for maximum PAE and maximum P_{out}, respectively. At both bias points the output power clearly decreases with increasing gate length for both epitaxial structures. This result does not correlate with DC measurements, where no dependency of the current on gate length was observed. As known from the literature [4], the difference in DC and RF results can be caused by current collapse phenomena. For the estimation of current collapse caused by gate lag, the drain current at a specific instantaneous bias point at V_{gs} = +1 V and V_{ds} = 10 V has been extracted, after pulsing the transistor from the two quiescent bias points. The current measured after pulsing from the quiescent bias point V_{gs} = -7 V, V_{ds} = 0 V has been normalized to the current obtained after pulsing from quiescent bias point V_{gs} = 0 V, V_{ds} = 0 V. Gate lagging conditions are emphasized by using this method. Fig. 3 shows the corresponding results. As can be seen from the graph, gate lagging shows the same fingerprint as load-pull measurements. The shorter the gate length the less gate lagging could be observed, consequently the RF output power increases with decreasing gate length. Thus, the observed large-signal performance is obviously strongly affected by a gate lag phenomenon. The detailed physical mechanism behind is still under investigation. One of the possibilities is trapping that is usually attributed to material quality or the interaction of the specific gate process with the material. In the future this factor will be experimentally studied by processing wafers with in-situ deposited SiN_x films. The second possible mechanism is due to a change of the piezoelectric polarization at different gate bias (inverse piezoelectric effect). The influence of both mechanisms, trapping and inverse piezoelectric effect increases with increasing Al concentration in the barrier. Barriers with high Al content may be prone to surface morphology degradation of the AlGaN layer [5] and to a reduced bulk quality of the material, which as a consequence might result in stability and reliability problems [6].

[1] A. Ashok, D. Vasileska, S. M. Goodnick, O. L. Hartin, "Importance of the Gate-dependent Polarization charge on the operation of GaN HEMTs," IEEE Trans. Electron Devices., Vol. 56, no. 5, May.2009

[2] G. H. Jessen , R. C. Fitch , J. K. Gillespie , G. Via , A. Crespo , D. Langley , D. J. Denninghoff , M. Trejo and E. R. Heller "Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-gate devices", IEEE Trans. Electron Devices, vol. 54, no. 10, pp.2589 -2597 2007

[3] O.Ambacher, J.Smart, J.R. Shealy, N.G. Weimann, K.Chu, M.Murphy, et al, " Two-dimensional electron gases induced by spontaneous and piezoelectric polarization changes in N-and Ga-face AlGaN/GaN heterostructures," J.Appl.Phys., vol.87, no.1, pp.334-344, Jan.2000

[4] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping Effects and Microwave Power Performance in AlGaN/GaN HEMTs," IEEE Trans. Electron. Devices. Vol. 48, pp. 465-471, March 2001.

[5] M Miyoshi, T Egawa, H Ishikawa, "Structural characterization of strained AlGaN layers in different Al content heterostructures and its effect on two-dimensional electron transport properties", J. Vac. Sci. Technol. B 23 (2005) 1527.

[6] E. Zanoni , M. Meneghini , A. Chini , D. Marcon and G. Meneghesso "AlGaN/GaN-based HEMTs failure physics and reliability: Mechanismsaffecting gate edge and Schottky junction", IEEE Trans. Electron Devices, vol. 60, pp.3119 -3131 2013