InAlN/GaN HEMTs over 100-GHz f_T with an improved Y-Gate process by an i-line stepper

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Abstract

We previously developed a Y-gate process with a conventional i-line stepper. The process enabled us to obtain a current gain cutoff frequency (f_T) of 70 GHz for InAlN/GaN high electron mobility transistors (HEMTs). In this study, we reduced both gate length (L_g) and over-gate length (L_{og}) to decrease a gate-source capacitance (C_{gs}). We obtained remarkable short L_g of 110 nm, as an i-line stepper process. And short L_{og} of 410 nm was also obtained. InAlN/GaN HEMTs were fabricated with this improved process realizing C_{gs} reduction of 36% compared to the previous process. As a result, f_T over 100 GHz was successfully achieved. This simple and low C_{gs} process is suitable for low cost production of high speed InAlN/GaN HEMTs.

1. Introduction

High-speed operations of a current gain cutoff frequency (f_T) over 100 GHz have been reported for InAlN/GaN high electron mobility transistors (HEMTs) with gate length (L_g) less than 100 nm [1–3]. However, complicated processes such as an electron beam lithography and a regrowth technology were necessary. Therefore, we have focused on low cost and simple technologies suitable for mass production. We previously demonstrated a 150-nm Y-gate process with a conventional i-line stepper [4]. The process enabled us to obtain f_T of 70 GHz for InAlN/GaN HEMTs. To achieve higher f_T, we tried to optimize the Y-gate process to decrease gate-source capacitance (C_{gs}) by reduction of L_g and over-gate length (L_{og}).

In this paper, we describe epi structures and the detail of the Y-gate process. Then, we show the evaluation data of InAlN/GaN HEMTs fabricated with this new process.

2. Epi structures

InAlN/GaN HEMT epitaxial layers were grown by metal-organic chemical vapor deposition on 100 mm high-resistance silicon substrates. The typical structure consists of an AlGaN buffer layer, a GaN buffer layer, an AlN interlayer and a lattice-matched InAlN barrier layer. Sheet resistance is approximately 280 Ω/sq.

A GaN cap layer is effective to reduce the gate leakage current (I_g) which is a major issue of InAlN/GaN HEMTs [5-6]. In our previous study, we demonstrated sufficient low I_g of 1.6×10^{-6} A/mm by introducing the GaN cap layer [4]. However introduction of the GaN cap layer sacrifices high transconductance (g_m). We have developed a new epitaxial growth technique which can maintain low I_g without the GaN cap layer. In this study, we used this non-GaN cap layer structure.

3. Y-Gate process

An overview of the Y-gate process flow is shown in Fig. 1. First of all, a 40-nm-thick SiN film was deposited on the surface by sputtering using electron cyclotron resonance plasma. Then, a photo resist (PR) pattern was obtained by a conventional i-line stepper. The PR pattern was shrunk by O_2 plasma. Next a 300-nm-thick SiO_2 film was deposited on the pattern by sputtering. The SiO_2 film adhering to the sidewall of the PR was removed by a buffered hydrofluoric acid (BHF) solution. Then the PR was lifted-off. In the previous process, L_g after this reverse gate process was 120 nm. After optimization of the PR shrinkage process, we could obtain L_g of 70 nm.

The SiO_2 film on the ohmic region was etched by a combination of Cl_2/BCl_3 reactive ion etching (RIE) and the BHF solution. Since an etching ratio of SiO_2 to SiN by the BHF solution is approximately 100, etching can be stopped at the SiN surface. Then the mask, which consists of two different PR layers, was used for electrode formation. An undercut shape,

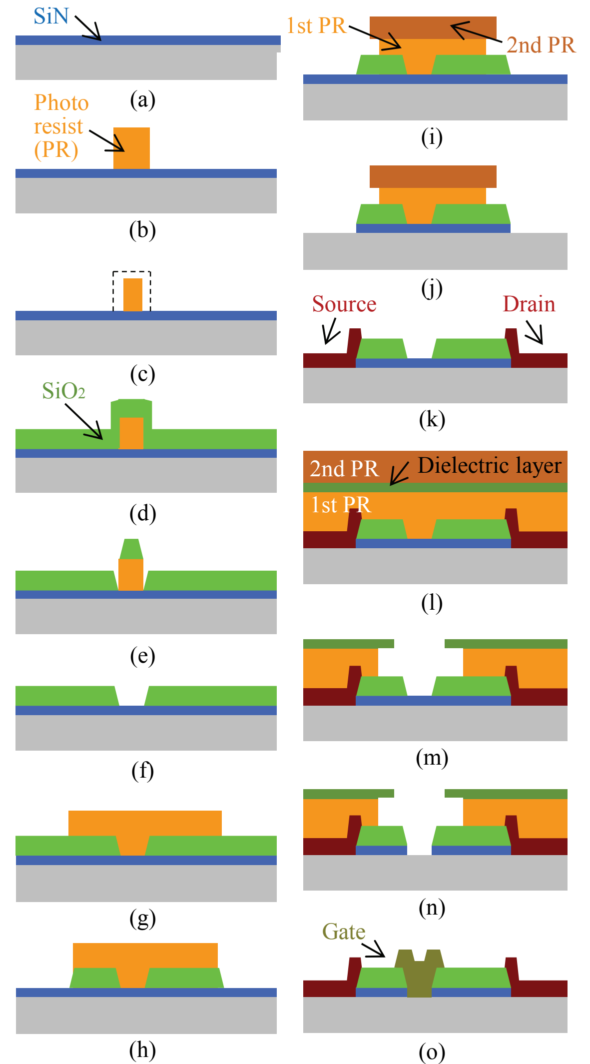

Fig. 1 Y-gate process flow.

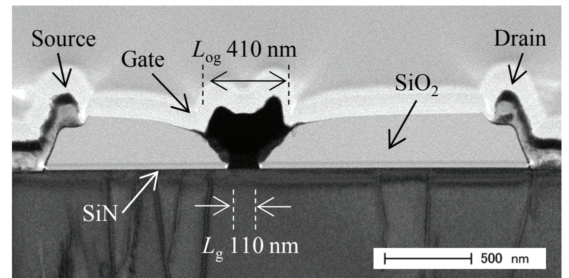

Fig. 2 Cross-sectional TEM image.

which helps lift-off process easier, was created as shown in Fig. 1(i). Then, the SiN film was etched by CF_4-RIE. Source and drain electrodes were formed on the InAlN barrier layer by a lift-off technique. Then, ohmic anneal was performed by a rapid thermal annealing.

Next, the mask, which consists of three different layers, was introduced to reduce L_{og}. A dielectric layer was sandwiched between 1st and 2nd PR layers. Opening region by three-layers-mask could be narrower than that by two-layers-mask. In addition, sufficient undercut shape could be obtained as shown in Fig. 1(m). Then, the SiN film on the gate was etched by CF_4-RIE. Finally, the gate electrode was evaporated on the surface and lifted-off.

A transmission electron micrograph (TEM) image of the cross section of the InAlN/GaN HEMT is shown in Fig. 2. L_g was 110 nm (150 nm in the previous process). L_g is a little longer than that after reverse gate process because L_g is enlarged at the final SiN etching (Fig.1(n)). L_{og} was 410 nm (600 nm in the previous process). We confirmed both L_g and L_{og} were successfully reduced. The gate sidewall was tapered and its angle was approximately 60º. We can control this angle by changing the SiO_2-thickness and RIE conditions. The angle is important, since it determines the parasitic gate capacitance and the electric field at the gate edge.

4. Evaluation

We measured the DC characteristics of the InAlN/GaN HEMTs fabricated with the improved Y-gate process. The drain and transfer characteristics are shown in Fig. 3. The evaluated deice has L_g of 110 nm, L_{og} of 410 nm and gate width (W_g) of 80 × 1 μm. The gate voltage (V_g) was swept from -3 to 2 V with 0.5-V-step. Maximum drain current (I_d) of 0.86 A/mm was observed. Even if InAlN barrier was applied, maximum I_d is relatively low because of thin barrier and high contact resistance. The on-resistance extracted at V_g at 2 V and drain voltage (V_d) in the range between 0 and 1.0 V was 1.8 Ωmm. Next, the transfer characteristics were measured at V_d of 10 V. Though the GaN cap was not applied, low I_g of 10^{-5} A/mm order was obtained. The peak g_m was as high as 490 mS/mm.

We measured the S-parameters using an Agilent 8510C network analyzer for the InAlN/GaN HEMTs with W_g of 50 × 2 μm from 10 to 80 GHz. After the pad parasitic was de-embedded, we extracted C_{gs} and g_m from an equivalent circuit model obtained from the measured S-parameters. L_g and L_{og} dependence on C_{gs} and g_m are shown in Fig 4. The highest g_m of 490 mS/mm was achieved at L_g of 220 nm. Short L_g is effective in reduction of C_{gs} remarkably. On the other hand, short L_{og} is also effective in reduction of C_{gs}. The lowest C_{gs} of 0.58 pF/mm was obtained at L_g of 110 nm and L_{og} of 410 nm. Since C_{gs} in the previous process was 0.90 pF/mm, we could reduce C_{gs} by 36%.

The gain characteristics are shown in Fig. 5. f_T of 110 GHz and maximum oscillation frequency (f_{max}) of 140 GHz were obtained under the bias condition of V_d of 10 V and I_d of 300 mA/mm. We could achieve over 100 GHz f_T, however, the f_{max} / f_T ratio was as low as 1.3. The reason of such low ratio is due to the high gate resistance because both L_{og} is short and electrolytic plating process is not applied. We believe much higher f_{max} shall be achieved by introduction of the electrolytic plating process.

5. Conclusions

We successfully improved the Y-gate process with C_{gs} reduction of 36% compared to the previous process. As a result, f_T was achieved over 100 GHz. This simple process with a conventional i-line stepper is suitable for low cost production of high speed InAlN/GaN HEMTs.

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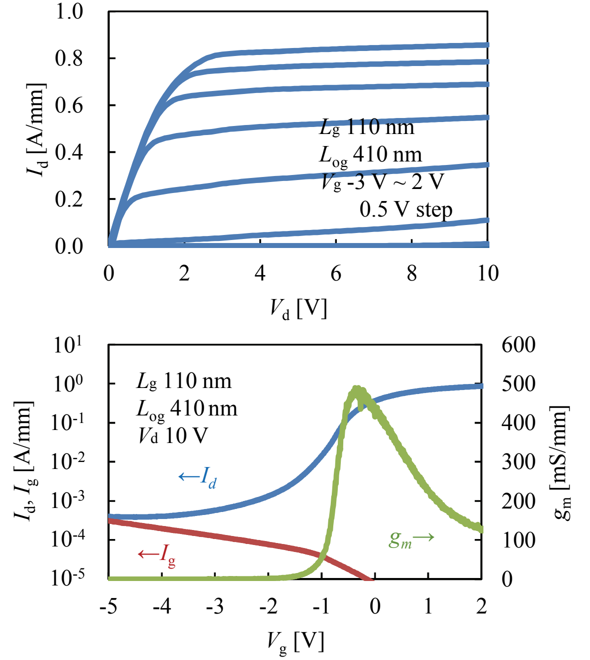

Fig. 3 Drain and Transfer characteristics.

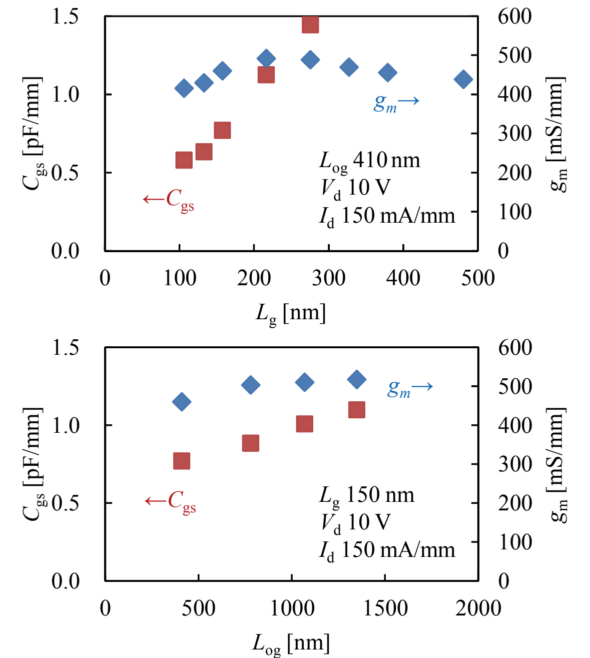

Fig. 4 L_g and L_{og} dependence on C_{gs} and g_m.

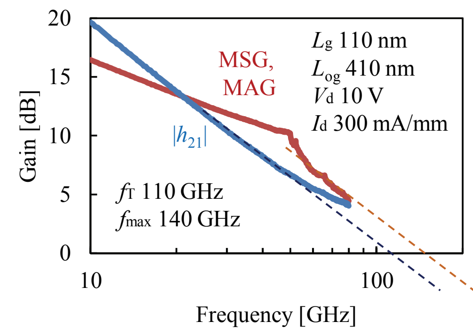

Fig. 5 Gain characteristics.