Improving Return on Invested Capital (ROIC) in PHEMT Technology

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INTRODUCTION

The semiconductor sector has been fairly volatile in the past three decades. When the PC market was expanding dramatically in the 90's, venture capital firms poured funding into semiconductor companies, and tech IPO's were regularly offered in NASDAQ. However in the recent years, venture capital has all but evaporated and the semiconductor sector has seen many consolidations, signaling that companies are facing ever increasing difficulties. A few notable examples are found here [1][2]. In these tumultuous times, many working in semiconductor fabs are asking why all this is happening and what were the main causes for this.

This paper will not try to answer these questions; instead we rely on experts that are well acquainted with the semiconductor sector---McKinsey Consulting. According to [3], the correct metric for evaluating semiconductor fab should be return on invested capital (ROIC), rather the typical metrics such as fab utilization or market share, or year-to-year revenue growth. ROIC takes account of the earning in context of the capital expenditure, whereas other metrics do not take in account the cost side of the equation. According to [3], while many firms have managed to secure funding for ever-more advanced fabs with greater capacity and at smaller lithography, few have managed to earn enough income to make the investment worthwhile. This is because while all capital expenditures (such as installing advanced tools or R&D of a new technology) are well-intentioned with attractive growths and profitability, it is difficult to predict their success due to the accuracy of market projections and competitors in this market. In fact the semiconductor industry has experienced many periods of oversupply. This has caused venture capital to seek more profitable investments elsewhere, and fabs that suffered losses faced shutdowns or acquisitions.

Recently, RFMD Greensboro fab has been actively finding ways to reduce cost and increase yields to improve ROIC. The motivation to seek more return on existing processes is felt throughout the organization. This paper seeks to document just a few yield improvement projects on our PHEMT technologies. We have 1) improved wafer uniformity with a different platen design, and 2) improved adaptive metal selection to fine-tune critical parameters at the product die. We use KGD and PCM data to show the yield improvements, and use ADS simulation to understand the sources of variation in circuits. In keeping with the philosophy of ROIC, we will estimate the potential benefit as well as the cost needed to achieve them, and evaluate their success individually. In order to make this industry-relevant, we created a "typical GaAs Fab" financial model using publically reported data on revenue, profit margin, etc. We conclude that the incremental ROIC, or the return on investment from these two projects are much higher than the industry standard, however ROIC of the overall fab has only slightly increased.

SECTION I: IMPROVED WAFER UNIFORMITY

The need for wafer uniformity improvement was first noticed in a particular mask where failed KGD die were always on the wafer edge (Figure 1).

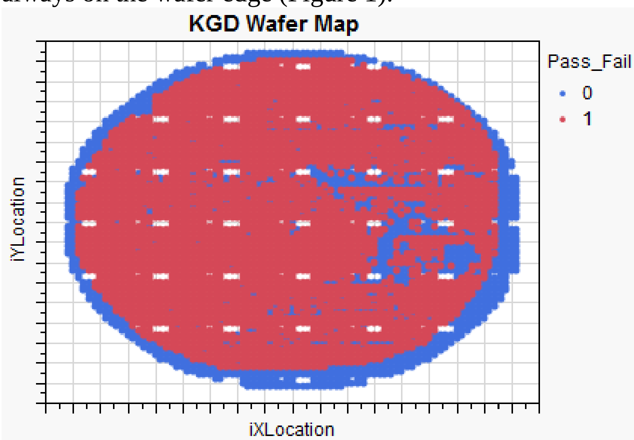

Figure 1. KGD map of a typical low-yield PHEMT wafer; red is passed die, blue is failed die.

We began a series of steps to understand this failure signature. First, we isolated the uniformity problem to the epi. Then we began a series of meetings with epi vendors, to bring this to their attention and worked with them to investigate the cause of epi non-uniformity. The various meeting spanning several months have resulted in many improvements. After some time when approximately a thousand wafers of new and old epi were run, the average yield increased by 2%. As we depleted the old epi, the overall yield continues to hold at this level. The epi growth improvements will be discussed more in the full paper.

SECTION II: THE MOTIVATION AND IMPLEMENTATION OF ADAPTIVE TOP METAL

With respect to yield improvement, sources of variation such as TFR, beta, or Vpo interact within the circuit to create a complex behavior; oftentimes it is desirable to focus on variations that have the most impact on final yield. ADS DOE [6] program allows one to quantify the impact of each source of variation; this will be discussed in more detail in the full paper.

The difficulty with yield improvement within the fab is that there are a diverse set of masksets, each with their own sensitivities. It is risky to re-center any process; for example, adjusting TFR might increase yield for some masks while decreasing yield for other masks. Process tightening is therefore highly desired, however moving to new processes also involve some amount of risks and engineering effort. At some point the process variation is due to fundamental limitations of the tools and materials being used, and further improvement requires new investments. As previously explained about the ROIC of fabs, new expenditure means increased invested capital and therefore additional income is expected. In order to increase ROIC we need to leverage as much as we can with existing tools and processes.

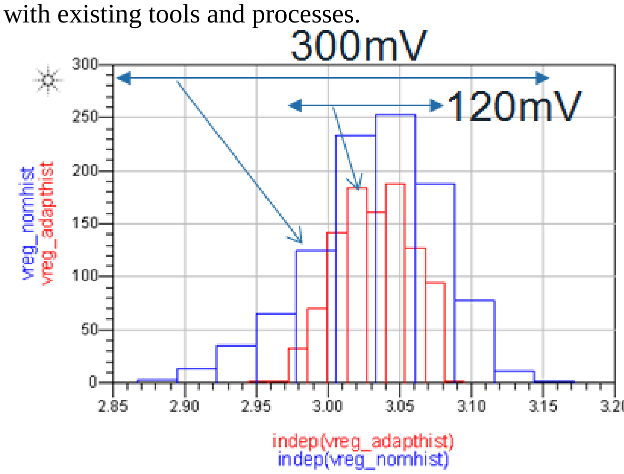

Figure 5. The effect of FET Gm on Vreg. Blue triangle is actual KGD data, red circle is Monte Carlo simulation.

A way we reduce variation with very little investment is the concept of adaptive mask. At first metal we have an idea whether a wafer is “high”, “nominal”, or “low” with respect to where it sits in the overall distribution, by electrical test of bias circuits at PCM. Then at top metal photo, there are multiple masks that we can choose from. We offer “high”, “nominal”, or “low” top metal masks for adaptive. The differences between these three masks is mainly the shorting or opening of certain resistors that can adjust the bias up or down. So depending on what value we measure at first metal, we will apply the top-metal mask that gives optimal yield. An example of this adaptive mask is shown in Figure 2, which shows that the regulator variation drastically reduced with adaptive top metal. Details of the implementation and simulation of adaptive mask is given in the full paper.

SECTION IV: DISCUSSION

In probably every technical paper the authors have read, the paper begins with stating the problem and then ends with problem solved or observations made. However, the “was it worth it?” questions were not always asked. Did the effort to arrive at the solution and the cost of the solution itself make sense financially? Let us estimate the impact on ROIC for the improved wafer uniformity project, and then the adaptive mask.

First we need manufacture statistics such as invested capital of the fab facility, wafer volume, price per wafer, processing cost, etc. Since proprietary company information can’t be discussed in the broad community, a “generic GaAs foundry” is created strictly based on conference publications and public filings. This foundry model will represent an “average” integrated device manufacturer (IDM), as a means to treat the fab as an independent unit and thus assess its financial strengths. There is no certainty in this way of analysis; the forecast numbers can be wrong, and broad estimations are sure to create errors. Nevertheless, this is still the common practice by financial analysts (for example, see [7,8]). It is better to have an inaccurate model based on best-guess estimates than to have no model at all. Using this “generic GaAs foundry”, the impact on ROIC for these two improvements will be analyzed in the full paper.

Section VII: Reference

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