# Orderly array of in-plane GaAs nanowires on exact (001) silicon for antiphase-domain-free GaAs thin films

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In the past few years, there has been a growing interest in the heteroepitaxy of III-V nanostructured materials on dissimilar Si substrates, aiming to provide the mainstream Si technology with III-V functionalities. At present, a great emphasis of the research has been directed toward selective area growth on pre-patterned Si using the aspect ratio trapping (ART) process [1-2], in which the defects originated from the large lattice mismatch presumably can be blocked by the dielectric sidewalls. Recent studies also suggest that use of a V-grooved Si (111) surface to the ART growth can be beneficial to restrict the generation of antiphase-domains and further enhance the defect trapping efficiency [3-4]. So far, high crystalline quality III-V channel materials for nanoscale transistors have been integrated on Si using this approach. However, the very small volume of useful materials in the growth cavities limits this technique in photonics device applications which typically require a larger active area [5]. In this work, we present the use of high density, orderly array of in-plane GaAs nanowires on exact (001) silicon to produce GaAs thin films with good crystalline quality, flat surface and no antiphase-domain boundaries (APDs). Such a growth scheme eliminates the need of using misorientated Si wafers and graded SiGe/Ge buffers in traditional blanket heteroepitaxy [6]. Due to the combined advantages from nanopatterned growth and epitaxial lateral overgrowth, low defect density, large-area GaAs thin films have been achieved on industrial-standard Si substrates.

N-type on-axis Si (001) substrates were used in the experiments. [110] direction aligned $SiO_2$ strip patterns with trench width of 90 nm and $SiO_2$ spacing of 40 nm were formed by top-down lithography and dry etching process. After surface cleaning using RCA-1 solution and native oxide removal by diluted HF, the sample was immediately immersed in a 45% KOH solution (70 ℃) to etch the Si surface. {111} facets were revealed at the bottom of the trenches as a result of the lowest Si etch rates in {111} planes. The material growth was carried out using a low-pressure metal-organic chemical vapor deposition system with a horizontal reactor. After a thermal cleaning step at 800 ℃ in the reactor, selective area growth of GaAs nanowires was performed using a two-step growth procedure that consists of a low-temperature (LT) nucleation layer and a high-temperature (HT) main layer, as illustrated in Fig. 1. Fig. 2 shows the tilted view SEM image of the closely pitched GaAs nanowires separated by the $SiO_2$ sidewalls. High position-controllability, good uniformity and smooth facets have been demonstrated. Fig. 3 displays a cross-sectional TEM image of the GaAs nanowires taken along the [110] zone axis. We found the lattice mismatch between the Si and the GaAs was accommodated within the initial few nanometers by stacking faults. The main body of the GaAs, on the other hand, shows high crystalline quality with very few defects. Prior to the coalesced thin film growth, the $SiO_2$ walls were removed by buffered oxide etch, and the resultant GaAs nanowire array was shown by the tilted view SEM image in Fig. 4(a). After overgrowth of a 60 nm GaAs layer, these high density nanowires have merged together (Fig. 4(b)), with the presence of bumpy surface morphology. A flat surface was reached after 300 nm GaAs overgrowth, as indicated by the cross-sectional SEM image in Fig. 4(c). Eventually, a 900 nm GaAs layer was grown on top of the nanowires for better crystalline quality (Fig. 4(d)). Fig. 5 shows the AFM image of the 300 nm coalesced GaAs layer. A root-mean-square value of 1.9 nm across a scanned area of $5\times5$ $\mu m^2$ has been achieved. We found spiral patterns related to dislocations and a few stacking faults appearing as straight lines, but no antiphase-domain boundaries were observed. The crystalline quality of the GaAs thin films was evaluated by high-resolution x-ray diffraction. Fig. 6 shows the ω-rocking curves measured from the 900 nm GaAs layer in Fig. 4(d) near the (004) reflection. The full-width-at-half-maximum (FWHM) values are 238 arcsec when the x-ray beam was aligned along the [110] direction and 310 arcsec when the x-ray beam was aligned along the [110] direction. The small linewidth of the x-ray diffraction and the antiphase-domain-free surface morphology suggest the great potential of using nanowire array to fabricate high quality GaAs-on-Si compliant substrates for monolithic integration of III-V devices on Si.

**Reference:**

[1] J. Li *et al.*, Appl. Phys. Lett, vol. 91, p. 021114, 2007. [2] R. Cipro *et al.*, Appl. Phys. Lett, vol. 104, p. 262103, 2014. [3] W.Guo *et al.*, Appl. Phys. Lett, vol. 105, p. 062101, 2014. [4] M. Paladugu *et al.*, Cryst. Growth & Des., vol.12, p. 4696, 2012. [5] N. H. Julian *et al.*, J. Cryst. Growth, vol. 402, p.234, 2014. [6] R. M. Sieg *et al.,* J. Vac. Sci. Technol. B, vol.16, p. 1471, 1998.

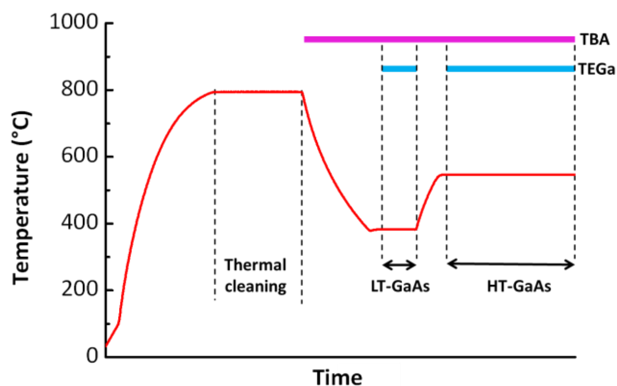


Fig. 1. Two-step growth procedure for selective epitaxial growth of GaAs nanowires on patterned Si (001) substrates.

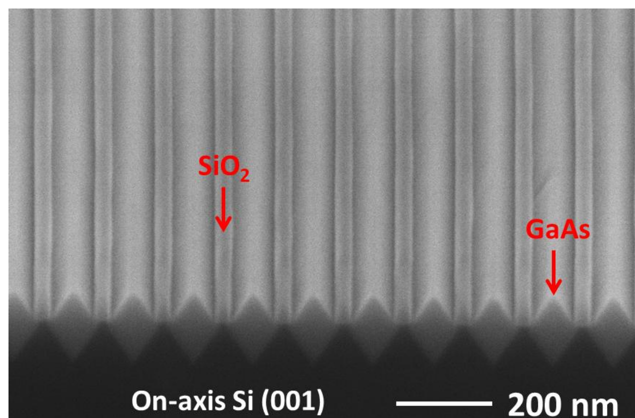


Fig. 2. Tilted SEM image of orderly array of GaAs nanowires.

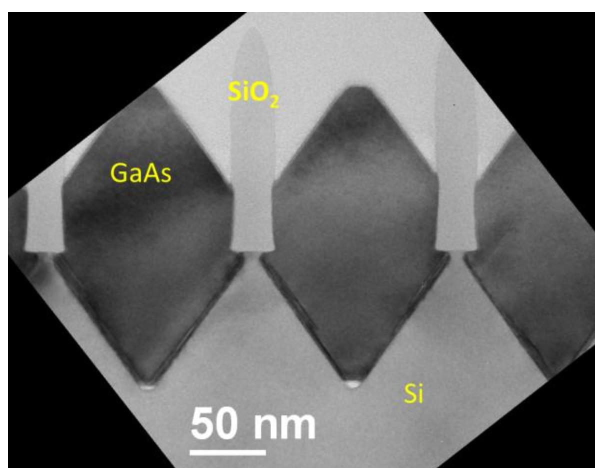


Fig. 3. Cross-sectional TEM image of the in-plane GaAs nanowires separated by $SiO_2$ sidewalls.

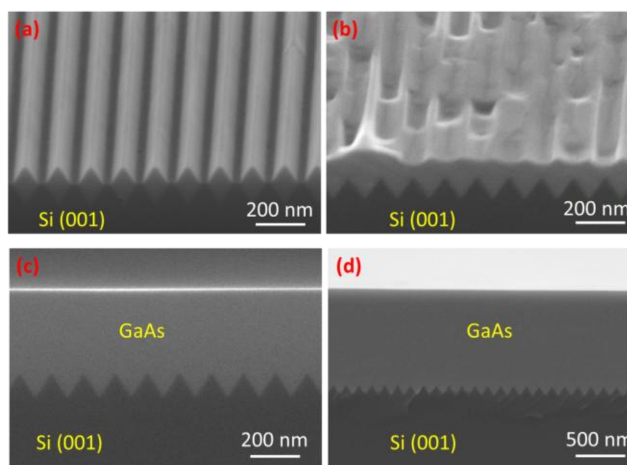


Fig. 4. (a): Tilted SEM images of GaAs nanowire array after $SiO_2$ removal; (b): Tilted SEM image after overgrowth of a 60 nm GaAs layer; (c): Cross sectional SEM image of 300 nm GaAs on nanowires; (d): Cross sectional SEM image of 900 nm GaAs on nanowires.

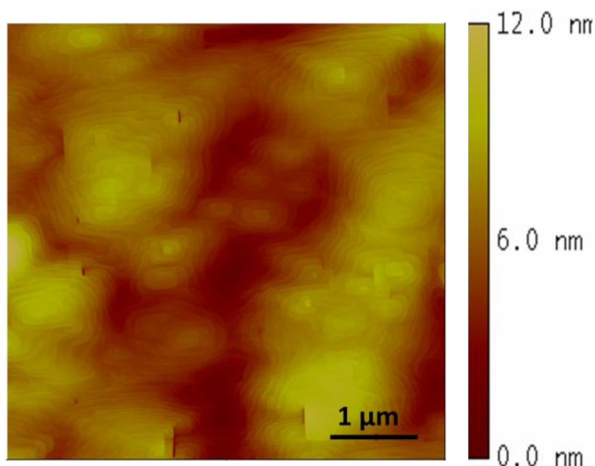


Fig. 5. AFM image of 300 nm coalesced GaAs thin film on nanowire array on Si (001) substrates.

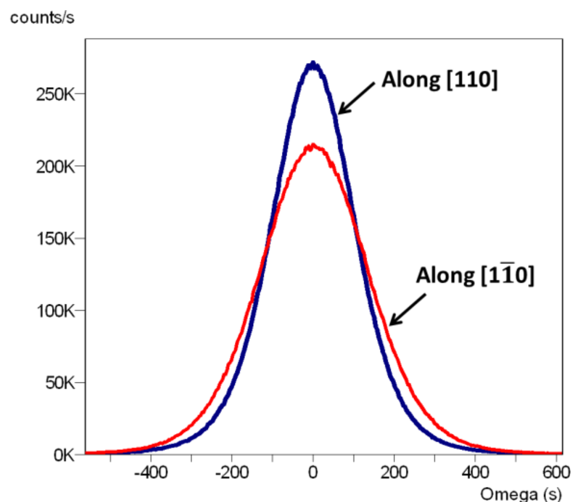


Fig. 6. XRD ω-rocking curves near the (004) reflection for the 900 nm GaAs layer on nanowire array on Si.