# High Aspect Ratio Individual Source Through Wafer Vias for High Frequency GaAs pHEMT Processes

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ABSTRACT

**Through wafer via holes play a major role for the III/V – semiconductor electronics. The GaAs etch processes for these high aspect ratio structures are well understood and applied. However the benefits of a slot via configuration for source connection of high power and high gain pHEMT processes in high frequency lead to a performance improvement of the transistor by reducing significantly the source inductance. In this work the process characterization of the dry chemical via hole etching in GaAs in terms of via slope and aspect ratio limitations will be discussed. Additional points rising benefits of the perpendicular via hole process compared to a tapered one regarding process stability and integration. The electrical characterization of these via holes as well the performance on a 150nm pHEMT power process will be shown. Hereby inductance extracted from S-parameter measurements on via modeling structures as well as on the new process technology PPH15X-20 of UMS.**

PURPOSE

The intent of this work is to provide information on:
1) Requirements on resist mask for chlorine dry chemical etches.
2) ICP etch process characterization investigating the etch rate, selectivity and slope of via in GaAs by applying a specified slot via pattern as test mask (figure 1).
3) Impact of via side wall roughness on metallization process.
4) How depend the via inductance on the via size and slope? Inductance measurements on modeling structures with varying pattern size as well as wafer thickness and via slope are compared.
5) Does the perpendicular via hole process with a slot via configuration improve the performance of the transistor technology PPH15X-20?

WHAT SPECIFIC RESULT WERE OBTAINED?

1) The resist mask slope can be stabilized by a fluorine insitu plasma before the chlorine etch.
2) figure 2 shows the etch rate depending on slot via hole size and aspect ratio. Selectivity and etch rate are characterizes depending on plasma parameters and via patterns. Additionally the etch rate decreases strong with reduced slot via length (figure 3).
3) Side wall quality depend on process pressure and RF bottom power that impacts the selectivity of GaAs to resist figure 4. Furthermore the slope of the perpendicular via hole depend on width of slot via and the process selectivity.
4) figure 5 – The roughness of the via side wall impacts more the conformity of the electroplated Au than the difference in aspect ratio of the via.
5) via inductance depend on the circumference of the via pattern at a certain via hole slope and wafer thickness - see figure 6.
6) The implementation of a slot via approach for the PPH15X-20 process technology show no impact on the Gain performance by exchanging the tapered vias by the perpendicular slot via holes. However the gate pitch can be reduced by this approach in order to optimize the transistor cell size regarding RF performances.

HOW COMPOUND SEMICONDUCTOR TECHNOLOGY WAS ADVANCED?

This work shows a detailed integration and evaluation of a process concept in a compound semiconductor manufacturing process. The via inductance reduction of around 10 pH for the source via connection of the transistor of a high gain and power technology can be shown. The source via inductance is reduced by increasing the circumference of the via without changing the transistor gate pitch size today. This goal is successfully reached by implementing the slot via pattern and a more reproducible via hole etching process. The methodology of this process development is a good example for the requirements of process integration work in compound semiconductor industry.

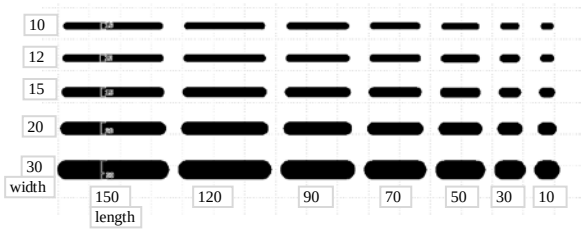


Figure 1 - slot via etch pattern for plasma process characterization (all values in µm)

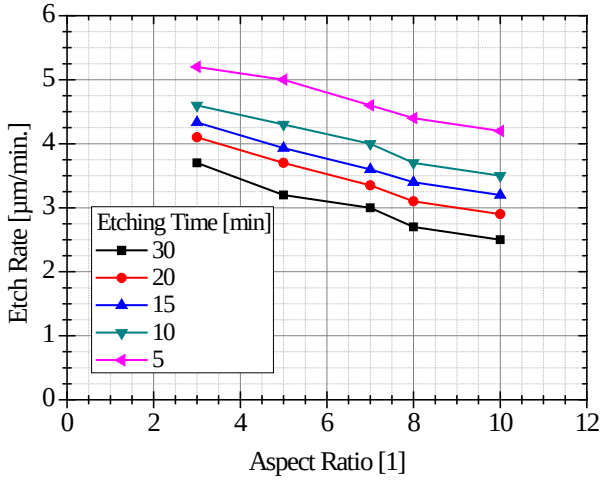


Figure 2 – GaAs etch rate on slot via patterns depending on Aspect ratio and etching time

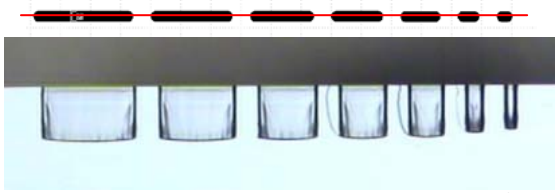

Figure 3 – cross section along the slot via holes at a width of 15µm

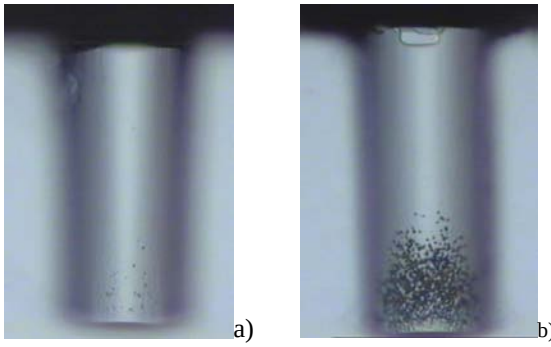


Figure 4: characterisation of side wall quality depending on GaAs to resist selectivity

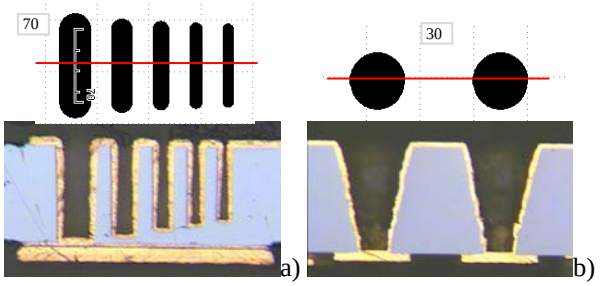


Figure 5 – metal conformity in slot via holes of 70µm in length a) compared to tapered vias of 30µm in diameter b)

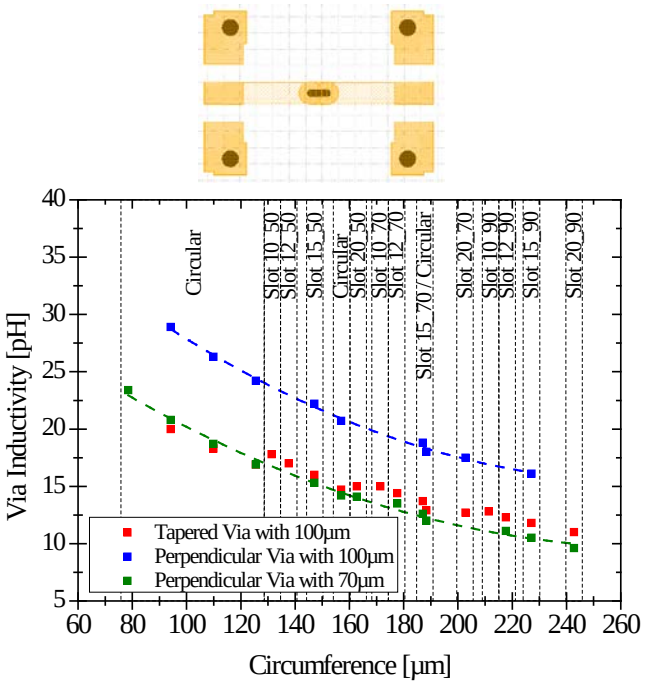


Figure 6 – extracted inductance from S-parameter measurements up to 40GHz (slot_width_length)

## REFERENCES

[1] H.Rubin, et al., The Effects of Increasing the Aspect Ratio of GaAs Backside Vias, 2012 GaAs MANTECH Technical Digest, pp. 103-107, CS MANTECH Conference, April 23rd - 26th, 2012, Boston, Massachusetts, USA

## ACRONYMS

ICP: Inductive Coupled Plasma

RF: Radio Frequency