

Effect of Gate Threshold Swings by ALD-Al₂O₃/AlGa_N Interfacial Traps in GaN Power HEMT with Multiple Fluorinated Gate Dielectric Layers

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Introduction: Normally-off AlGa_N/GaN HEMT is desirable in power applications in terms of system controllability. Fluorine ion (F⁻) treatment [1] and AlGa_N barrier recess [2] on the gate region are two of the approaches to deplete the carriers within the normal 2DEG conduction channel in normally-on HEMT. However, for conventional F⁻ treatment on AlGa_N surface [1], annealing was required after treatment for damage recovery which resulted in the escape of F⁻ and reduced V_{TH}. Unannealed multiple F⁻ treatments on AlGa_N surface and ALD-Al₂O₃ gate dielectric combining with partial AlGa_N recess reported in [3] allowed high total amount of F⁻ incorporation at the gate which resulted in a high V_{TH} of +5V.

Purpose and Significance of Work: This work attempts to analyze the Al₂O₃/AlGa_N interfacial quality of annealing-free device with 3 rounds of CHF₃-based F⁻ treatments within 4 layers of Al₂O₃ gate dielectric in HEMT which is expected to have good channel conductivity and high V_{TH} at the same time. Benchmarking with devices that underwent pre-fluorination annealing right after 1st layer of Al₂O₃ deposition, unannealed device has about 10 times lower shallow interface trap density (D_{it}) which resulted in significantly smaller drain leakage current. However, doubled Ultra-violet (UV) -assisted V_{TH} hysteresis (ΔV_{TH}) found in bi-directional I_D-V_G sweep indicates higher concentration of deep-level traps without gate stack annealing.

Results and Discussion: The device fabrication begins with Ti/Al/Ni/Au (25/125/45/55 nm) ohmic contacts formed by RTA at 850°C for 30s. Then, 500nm-deep mesa isolation is formed by BCl₃-based ICP-RIE and 150nm SiO₂ dielectric deposition by PECVD. After gate opening at the normally-off region, about 10nm of AlGa_N (50% in thickness) was recessed by low power BCl₃-based ICP-RIE to reduce the 2DEG concentration without damaging the AlGa_N/GaN interface that degrades mobility. After 6.5nm of ALD-Al₂O₃ deposition at 250 °C and different post-deposition annealing temperatures for gate recess recovery used on Dies B and C, 3 cycles of CHF₃ plasma treatment combining with ALD-Al₂O₃ were used for gate stack formation to introduce sufficient F⁻ charges in the gate region for high V_{TH}. Longer treatment period was applied on the top layer to minimize F⁻ penetration into the 2DEG channel that may create mobility degradation. Considering the CHF₃ plasma etching on Al₂O₃, the total Al₂O₃ thickness of 18.1nm is obtained. Detailed device schematics, SEM of the gate cross-section and gate process parameters are shown in Fig. 1 and Table I. The equivalent F⁻ sheet concentration of each layers was obtained by fitting the measured V_{TH} with Setaurus TCAD simulations.

Fig. 2 (a) shows the bi-directional transfer characteristics (sweep time=20s) of Dies A~C at V_D=8V comparing with D-mode MIS-HEMT with Al₂O₃ of 18nm without any gate recess. Slight increase of V_{TH} in positive sweep were found with annealing, shows formation of fixed negative charge after annealing. Additionally, different degree of positive shift in V_{TH} was observed during negative sweep, indicating trapping of electrons at the Al₂O₃/AlGa_N interface or Al₂O₃ bulk after applying high gate bias. Halved ΔV_{TH} was observed after annealing, proving effective reduction in deep-level

Al₂O₃/AlGa_N interfacial trap charge (Q_{it}). Shown in Table II are Q_{it} for Die A~C based on Fig. 2(a) along with the Q_{it} after 10s of UV-illumination (UV wavelength=365nm) to measure even deeper Al₂O₃/AlGa_N traps. Q_{it} were extracted based on [4] where $Q_{it} = \epsilon_0 \epsilon_{Al_2O_3} \Delta V_{TH} / (q t_{Al_2O_3})$, where $\epsilon_{Al_2O_3} = 7$, ϵ_0 is the permittivity in vacuum, q is the electronic charge and $t_{Al_2O_3}$ is the thickness of Al₂O₃ which is shown in Table 1. The bi-directional I_D-V_G in log-scale and I_G-V_G shown Fig. 2(b) has demonstrated increased drain leakage current under similar gate leakage after annealing.

Fig. 3 (a) compares the DC and pulsed I_D-V_D characteristic of Dies A-C at gate overdrive voltage (V_{GT} = V_G - V_{TH}) of 10V. For Pulsed I_D-V_D, it was measured with V_G pulse at -30V for 50ms and 50% duty cycle to examine the current collapse effect due to deep-level electron trapping from gate injection. High I_DMAX of 350mA/mm from unannealed Die A under steady state has shown good preservation of 2DEG mobility from CHF₃ plasma treatment. Worse current collapse effect obtained from the pulsed I-V measurement for Die A compared with Die B and C shown Fig. 3 (b) agrees with the higher amount of deeper level traps shown in Table II.

Fig. 4 shows the Al₂O₃/AlGa_N interface trap density (D_{it}) distribution from the AlGa_N E_V edge obtained from AC conductance method using $D_{it} \approx 2.5(G_p/\omega)_{max}/(Aq)$ [5], where (G_p/ω)_{max} is maximum value of the ratio between the parallel conductance (G_p) and the frequency in radians (ω) at each measured frequency, and A is the area of the gate. Annealing would increase the shallow trap level (E_T) density near the E_C edge, while the deeper-level Q_{it} obtained before (E_T=0.6eV based on 20s I_D-V_G sweep rate) and after (E_T=2eV, mid-gap of AlGa_N) UV illumination with wavelength of 365nm for 10s shown in Table II decreases with raised annealing temperature.

Fig. 5 explains the effect of carrier trapping & de-trapping mechanisms on ΔV_{TH} through schematic energy diagram. In Fig. 5 (a) when V_G=0V, holes accumulated at AlGa_N/GaN interface will be trapped at the shallow Al₂O₃/AlGa_N trap levels and hopping across the gate region into the channel induces drain leakage current. As more shallow level were found for annealed dies shown in Fig. 4, greater drain leakage current for Dies B & C shown in Fig 2(b) could be explained. When V_G>V_{TH}=V₁ in positive sweep shown in Fig. 5(b), electrons from 2DEG will be trapped at Al₂O₃/AlGa_N interface. Those trapped electrons will be slowly de-trapping back into 2DEG during negative sweep and those charges remained at the Al₂O₃/AlGa_N interface will deplete the 2DEG that causes positive V_{TH} shift under the same gate bias V₁ shown in Fig. 5(c). Thus, a higher amount of deep-level traps will result in greater trapped charges and larger ΔV_{TH} during the negative sweep.

Reference

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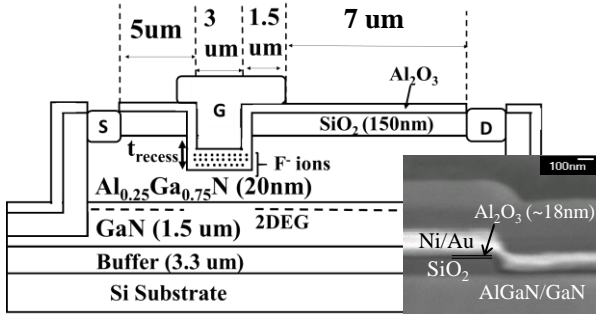
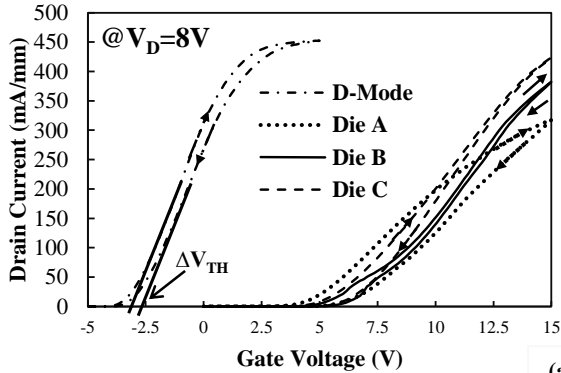


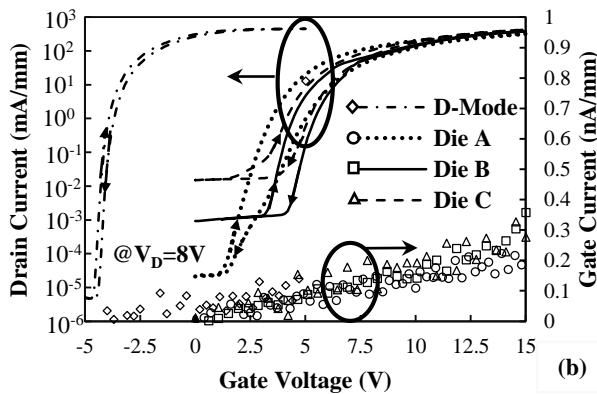
Fig. 1 Cross-sectional schematics and SEM image of the fabricated device

Table I. Steps for gate fabrication of Dies A~C

Steps	Process	Dies		
		A	B	C
1	ALD-Al ₂ O ₃	6.5 nm		
2	Rapid thermal annealing	N/A	500 °C in N ₂ for 60s	600 °C in N ₂ for 60s
3	F ⁻ treatment	CHF ₃ RIE @ 30W for 140s F ⁻ Conc. ~ -6.51 × 10 ¹² cm ⁻²		
4	ALD-Al ₂ O ₃	7.3 nm		
5	F ⁻ treatment	CHF ₃ RIE @ 30W for 260s F ⁻ Conc. ~ -1.21 × 10 ¹³ cm ⁻²		
6	ALD-Al ₂ O ₃	7.6 nm		
7	F ⁻ treatment	CHF ₃ RIE @ 30W for 280s F ⁻ Conc. ~ -1.30 × 10 ¹³ cm ⁻²		
8	ALD-Al ₂ O ₃	8 nm		
Total Al₂O₃ thickness considering F⁻ treatment etching (nm)		18.1 nm		



(a)



(b)

Fig. 2 (a) Bi-directional transfer characteristic of Dies A-C with benchmarking D-mode device in linear scale. The sweep was done in clockwise direction in 20s and threshold voltage hysteresis (ΔV_{TH}) is demonstrated. (b) Bi-directional transfer characteristic in logarithmic scale and I_G - V_G characteristics of Dies A-C and D-mode device. Low gate leakage current has ensured the preservation of insulation quality of the gate dielectric with fluorine treatments.

Table II. Extracted threshold voltage hysteresis and Al₂O₃/AlGaIn interfacial trap of Dies A~C.

Dies		D-Mode	A	B	C
V_{TH} in positive sweep (V)		-3.0	4.8	5.4	5.5
w/o UV	ΔV_{TH} (V)	0.4	1.4	0.75	0.5
UV	Q_{it} (10 ¹² cm ⁻²)	0.86	3.01	1.61	1.08
UV for 30s	ΔV_{TH} (V)	0.4	2.0	1.25	1.00
	Q_{it} (10 ¹² cm ⁻²)	0.86	4.40	2.72	2.20

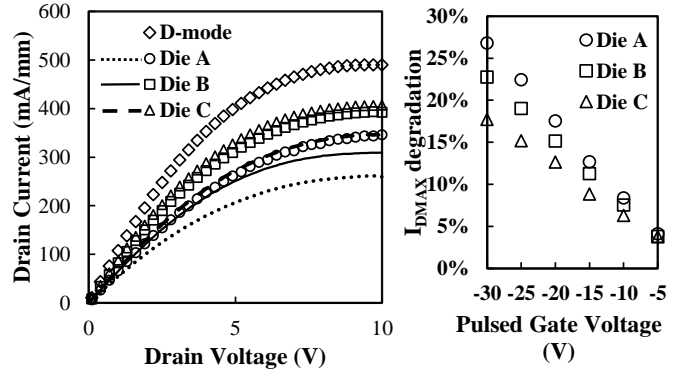


Fig. 3 (a) I_D - V_D characteristic of Dies A-C with benchmarking normally-on device at gate drive voltage in excess of V_{TH} (V_{GT}) of 10V in DC state (datapoints). Pulsed I_D - V_D (solid line) measured with V_G pulse at -30V for 50ms and 50% duty cycle is also included. High I_{DMAX} of 400 mA/mm was found for Die C, showing effectiveness of annealing on mobility restoration; (b) The amount of I_{DMAX} degradation for pulsed I-V measurement compared with DC I-V results at different pulsed gate voltage. Alleviation in the current collapse effect is found for Die C.

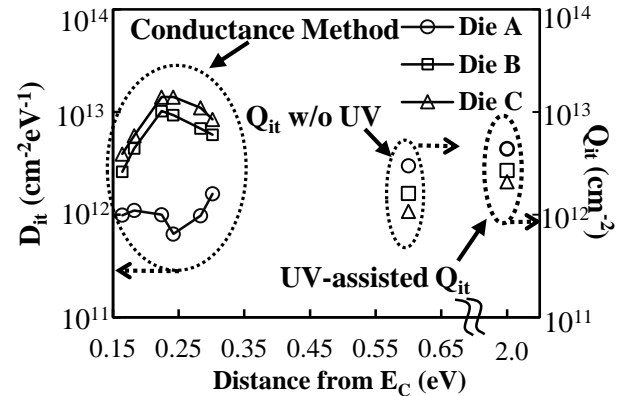


Fig. 4 Al₂O₃/AlGaIn interface trap density (D_{it}) distribution within the AlGaIn energy band obtained from conductance method ($E_T=0.165$ eV to 0.3 eV) and trapped interface charge Q_{it} from Bi-directional transfer characteristics before ($E_T=0.6$ eV based on 20s I_D - V_G sweep rate) and after 10s UV lamp illumination ($E_T=2$ eV) shown in Table II.

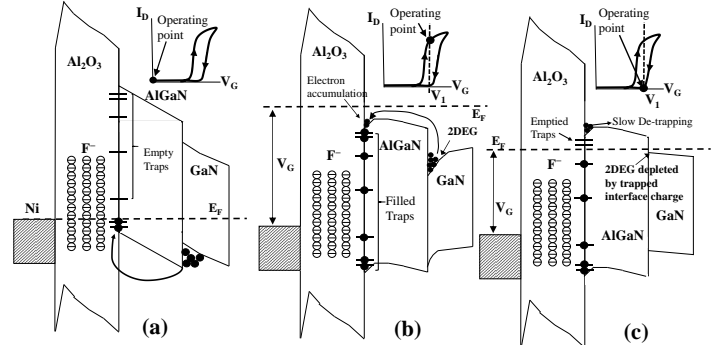


Fig. 5 Schematic energy band diagram of Al₂O₃/AlGaIn/GaN interface at (a) $V_G=0V$ (leakage current induced by hole trapping in shallow D_{it} and hopping across the gate region into the channel) (b) $V_G=V_1$ in positive sweep (trapping of Q_{it} from 2DEG) and (c) $V_G=V_1$ in negative sweep (2DEG depletion from Q_{it} resulted in positive V_{TH} shift)

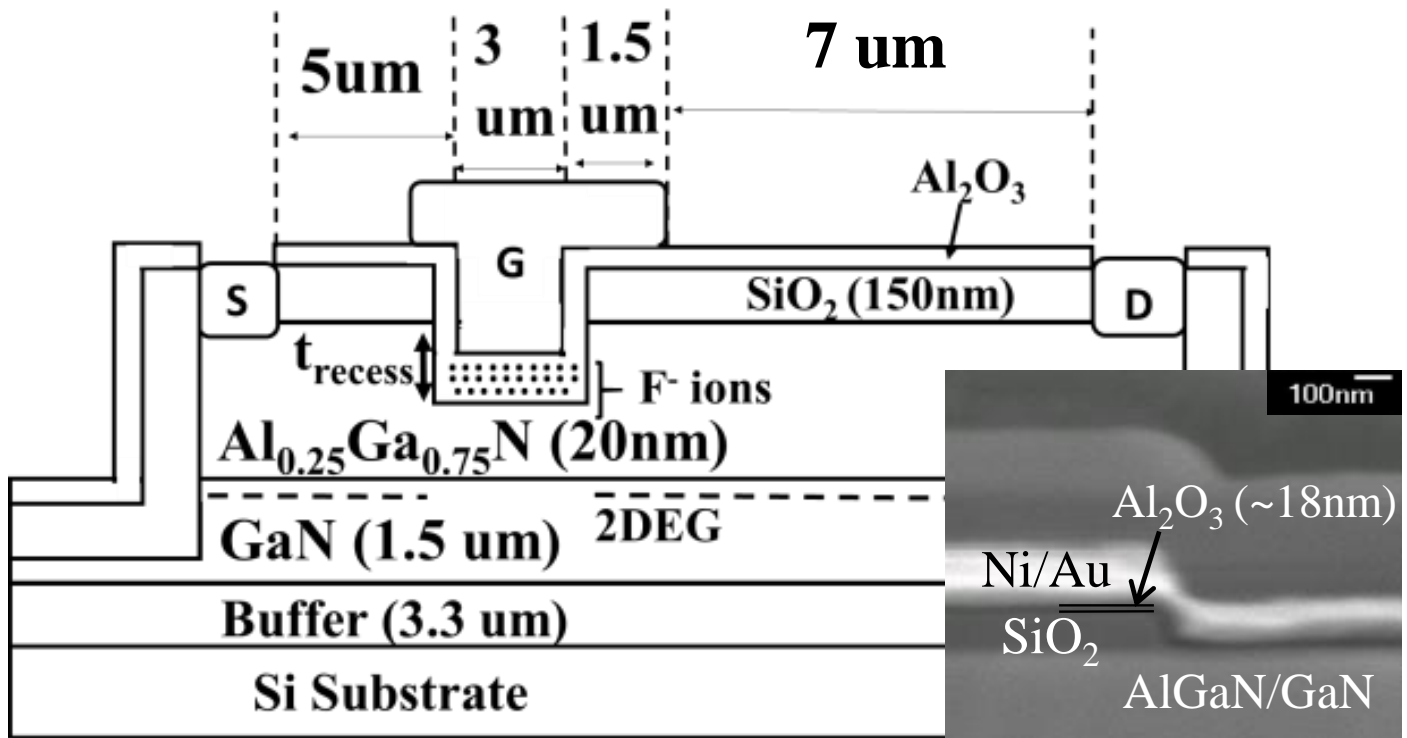


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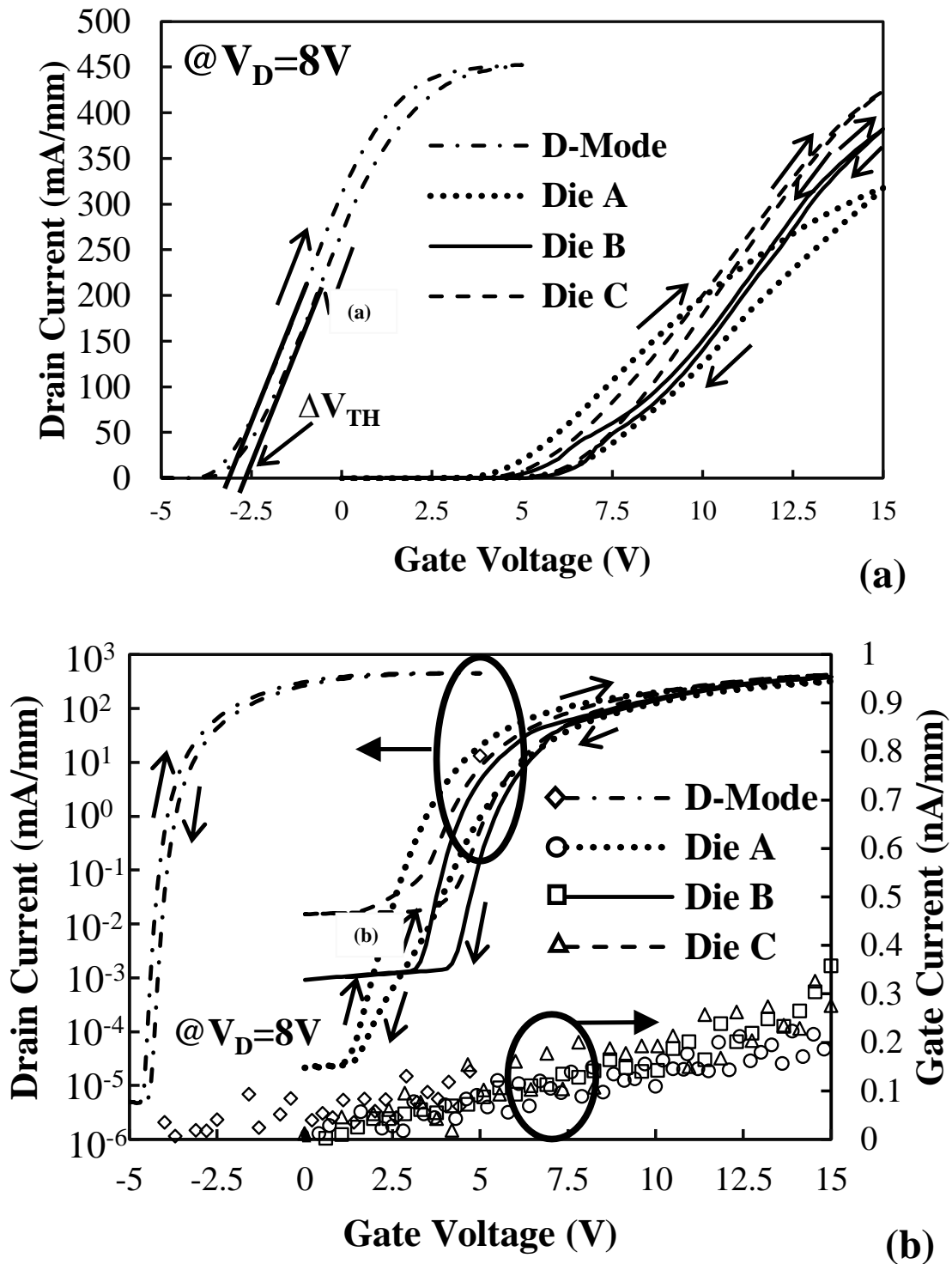


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Dies		D-Mode	A	B	C
Avg. V_{TH} (V)		-3.0	6.25	6.5	6.0
w/o UV	ΔV_{TH} (V)	0.4	1.4	0.75	0.5
	Q_{it} (10^{12} cm^{-2})	0.86	3.01	1.61	1.08
UV for 10s	ΔV_{TH} (V)	0.4	2.0	1.25	1.00
	Q_{it} (10^{12} cm^{-2})	0.86	4.40	2.72	2.20
RMS surface morphology of pre-fluorinated Al ₂ O ₃ obtained from AFM (nm)		N/A	0.65	0.50	0.30

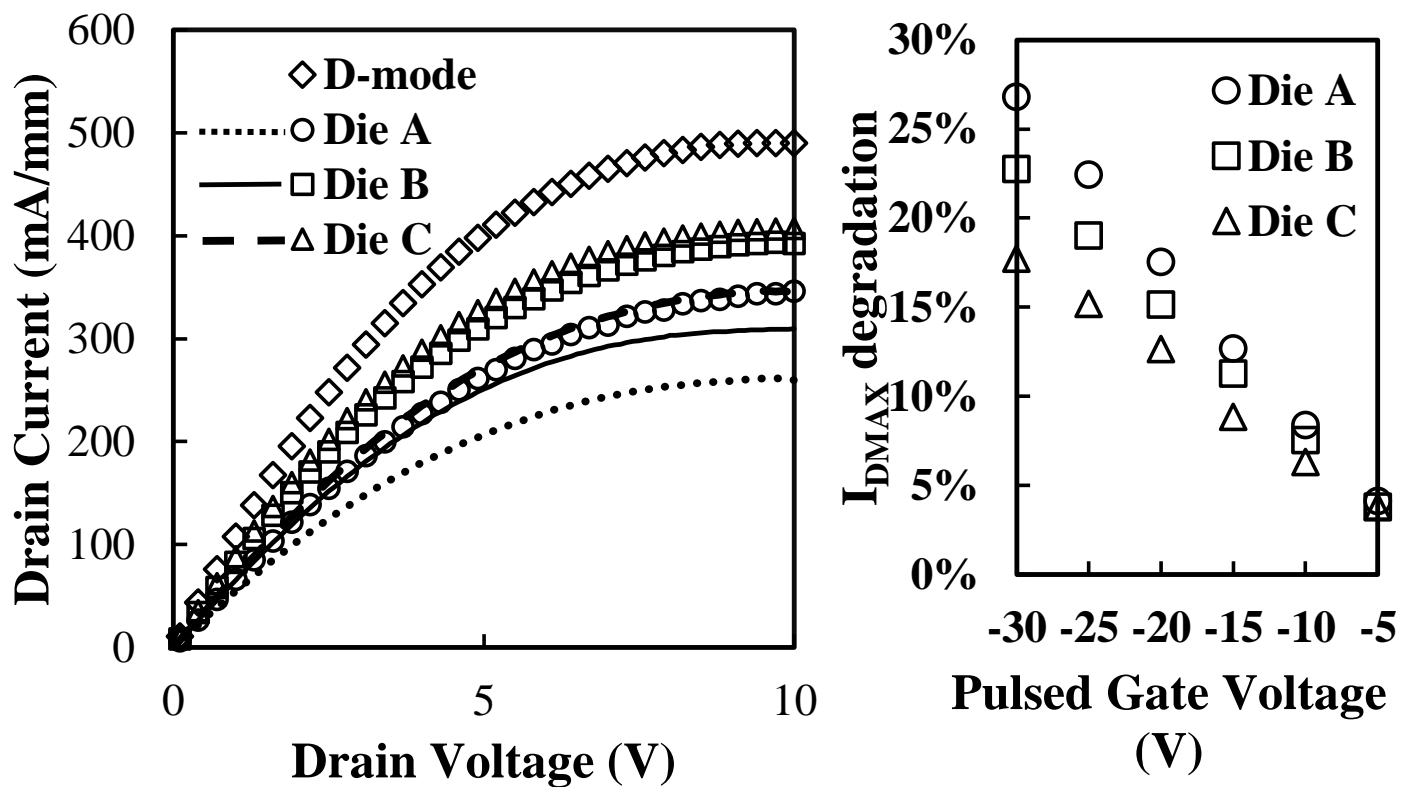


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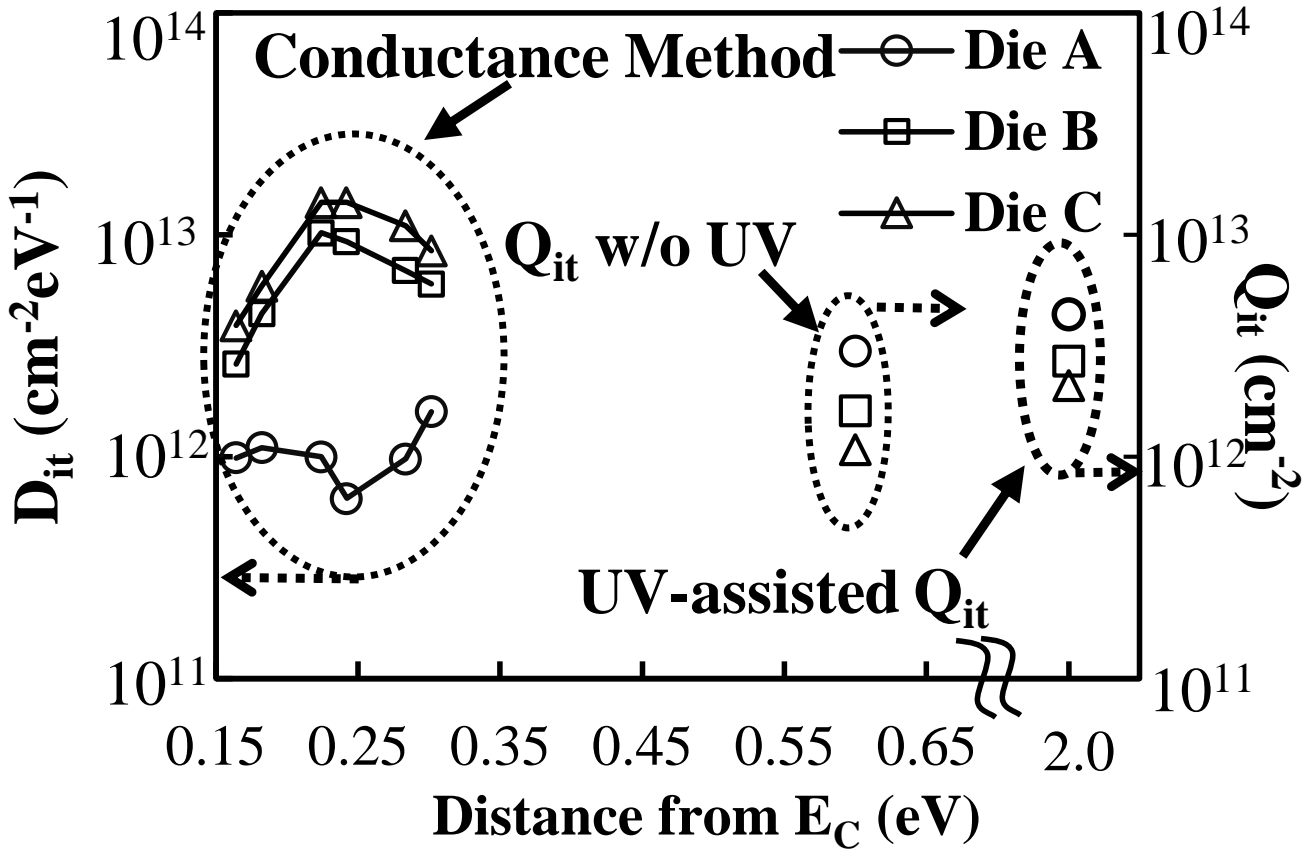


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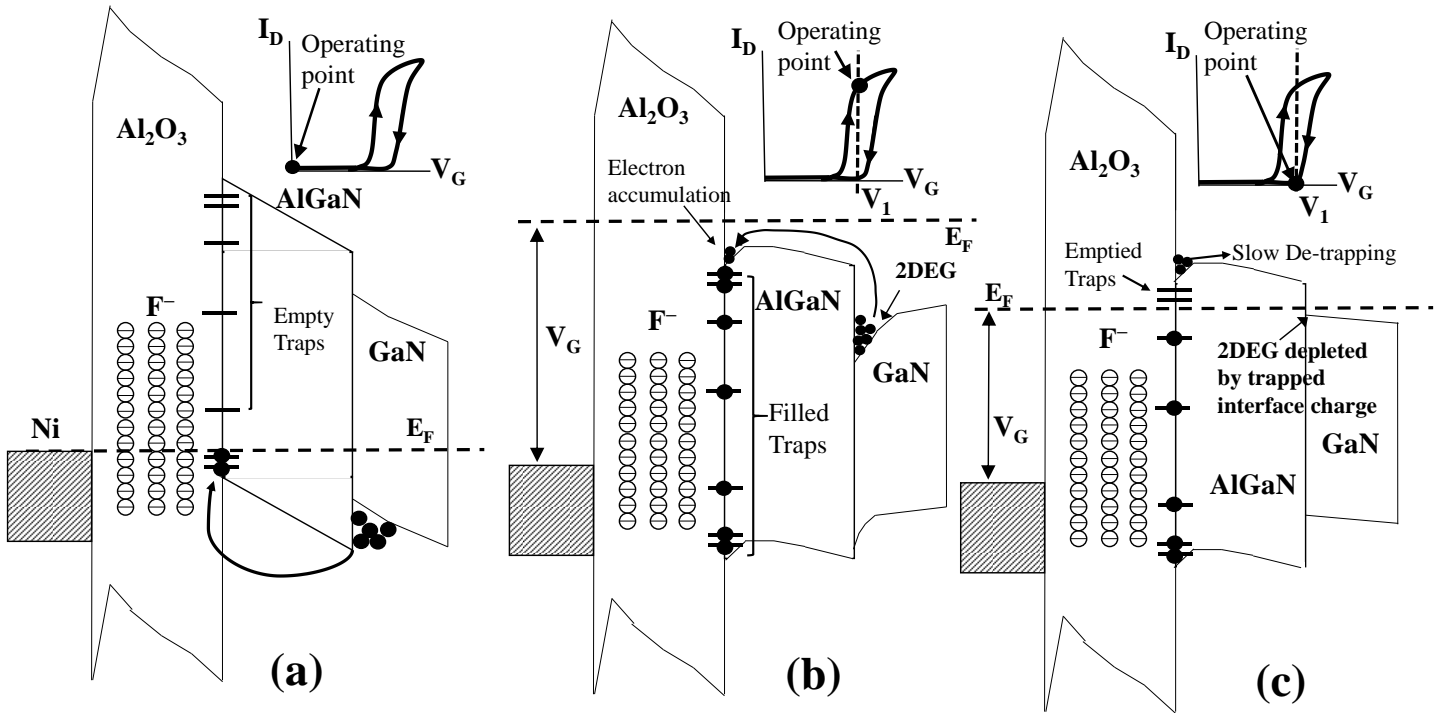


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