Simulation of the Impact of Through-Substrate Vias on the Thermal Resistance of Compound Semiconductor Devices

Rajesh Baskaran, Allen W. Hanson
MACOM Technology Solutions Inc., 100 Chelmsford St., Lowell, MA 01851
Telephone: (978) 656-2762
E-mail: rajesh.baskaran@macom.com

INTRODUCTION

MACOM is fortunate to have one of the broadest power transistor technology portfolios in the industry today including devices based on Si, GaAs, GaN-on-Si and GaN-on-SiC materials systems. While each of these technologies offer unique benefits with in the performance-cost trade space, a challenge common to all is the requirement that operational temperatures be maintained at levels that can assure long-term reliability of these components. Consequently, significant engineering time and attention are applied to thermal design. On the performance side, the use of through-substrate vias to achieve increased gain by way of lowering ground inductance is commonly applied throughout the industry. But this technique has the potential to degrade thermal performance depending upon the details of via configuration and construction, as well as the material system employed. In this paper, the results of a thermal simulation study are presented in which the cases of no via (baseline), via and solid-fill via are compared and contrasted for thermal impact in three different material systems of significance to modern power transistors; GaAs, GaN-on-Si and GaN-on-SiC. The impact of various via configurations, or styles, are also considered; end vias - those that reside outside the transistor cell active region, slot vias - those that make direct contact with transistor source contacts, and block vias - similar to slot vias, but extending the full length of the source contact.

APPROACH

For this work, thermal simulations were performed using ANSYS to conduct three dimensional finite element analysis. A field effect transistor layout featuring 42 fingers with a total gate width of 15.4mm and a gate-to-gate pitch of 50μm was chosen for the comparative study. Overall die size was fixed at 2.6 x 9.4mm and die thicknesses were fixed at 75μm for all cases. Temperature dependent thermal conductivity was taken into account for all of the semiconductor materials within the stack including epitaxial layers [1], and the impact of epitaxial interfaces was also considered [2]. Front-side interconnect metallization was deemed inconsequential for the purposes of this comparative study and was not included. Die were mounted to flanges comprising of copper-molybdenum-copper (CMC) materials and attached by AuSn eutectic with an associated bond line thickness of 38μm. For all cases in this study the 5.8x20.3mm flange was attached to an idealized heat sink maintained at 80°C. Simulations were performed at 55W (3.57W/mm) dissipated power for the GaN material cases, and GaAs devices were simulated at dissipated power level commensurate with the capabilities of this technology - 15.4W (1W/mm).

Simulations were validated by way of thermal imaging acquired using a Quantum Focus Infrascope 2 system on devices under DC operation. Figs. 1 and 2 show that the measured vs. modeled results compared favorably with the experimental IR image registering a peak temperature of 206.5°C, while the simulated equivalent yielded a peak temperature of 204.0°C. The associated thermal resistances are 2.30, and 2.25°C/W respectively. For the various cases investigated, three via types were considered; a 50μm diameter circular end via (Fig. 3a), a 20x40μm slot via (Fig. 3b.) and a 30x380μm block via (Fig. 3c). Additionally, three configurations were modeled: no-via (baseline) (Fig.4a.), no-fill via (Fig 4b.), and filled via (Fig. 4c.) where gold was used for the fill material. For the no-fill case, we assumed a zero thickness sidewall metallization to establish worst case impact of via cavity on thermal resistance.

RESULTS & DISCUSSION

The impact of end vias was found to be negligible for the GaN-on-SiC materials system for both the fill and non-fill cases – all temperatures falling within 1°C for each of the cases investigated. At the other configuration extreme, block vias resulted in significant interplay with the thermal resistance of the cell. For the GaN-on-SiC case it was found that no-fill configuration results in a 13°C increase in peak temperature over the baseline case, whereas filling these same vias essentially compensates for via insertion - not surprising given the similarity of SiC and Au thermal resitivities. Keeping in mind this is a worst case assessment, the results suggest via fill is of limited benefit to devices in this materials system. For the lower conductivity materials – the impact of block vias on thermal impedance is, however, far more significant. For the GaAs and GaN-on-Si systems, filling block vias resulted in a 44 and 48°C reduction in peak temperature respectively for the power density and layout configuration of this study – see Table I. While these gains are not insignificant, they need to be considered in light of the added cost and complexity associated with fill processes.

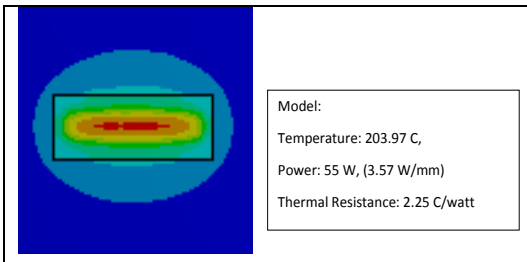

Fig 1. Isothermal plot of temperature for simulated case. Peak temperature is 203.9°C, and R = 2.25°C/W.

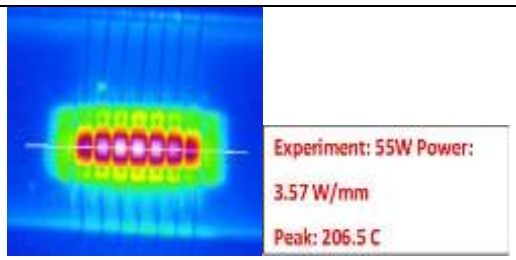

Fig 2. Isothermal plot for device measured using IR camera. Peak temperature is 206.5°C, and R = 2.3°C/W.

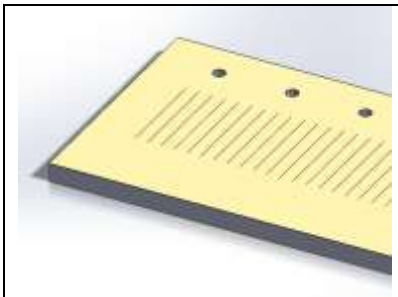

Fig 3a. Illustration of 50µm diameter end via configuration.

Fig 3b. Illustration of 20x40µm slot via configuration.

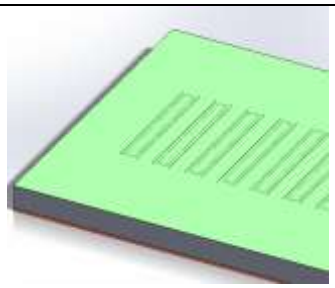

Fig 3c. Illustration of 30x380µm block via configuration.

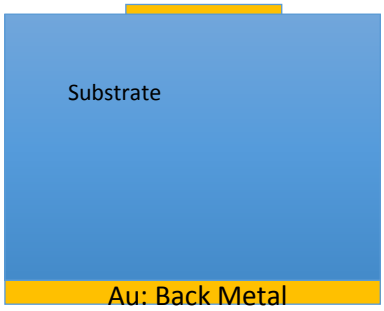

Fig 4a. Illustration of no via (baseline) case.

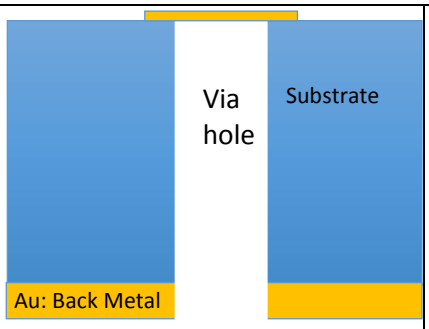

Fig 4b. Illustration of no-fill case.

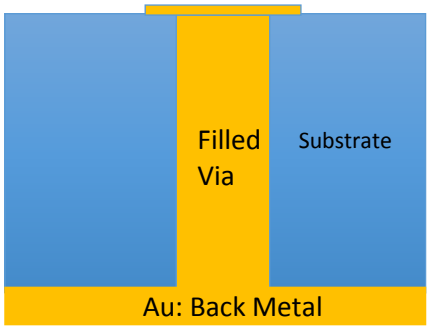

Fig 4c. Illustration of filled via case.

TABLE I

COMARRISON OF NO-VIA, NO-FILL, AND FILLED CASE TEMPERATURES

Materials System	No-Via Case (Baseline) (°C)	No-Fill Case (°C)	Fill Case (°C)	Temperature Delta Fill vs. No-Fill (°C)
GaN-on-SiC	201	214	197	17
GaN-on-Si	236	262	214	48
GaAs	153	170	126	44

REFERENCES

1. Hiroyuki Shibata, Yoshio Waseda, Hiromichi Ohta, Kazumasa Kiyomi, Kenji Shimoyama,Kenji Fujito, Hirobumi Nagaoka, Yuji Kagamitani, Rayko Simura; and Tsuguo Fukuda, "*High Thermal Conductivity of Gallium Nitride (GaN) Crystals Grown by HVPE Process"*, Materials Transactions, Vol. 48, No. 10 (2007) pp. 2782- 2786.

2. Jungwan Cho, Elah Bozorg-Grayeli, David H. Altman, Mehdi Asheghi, and Kenneth E.Goodman, *"Low thermal Resistances at GaN-SiC interfaces for HEMT technology " IEEE Electron Device Letters, VOL. 33, NO. 3, March 2012.*