Characterization of strained AlGaN/GaN HEMTs on CMP-thinned Si substrates

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III-Nitride high electron mobility transistors (HEMTs) on large area, low cost Si substrates have attracted much attention from the commercial RF device community due to steady advances in epitaxial growth, material quality, and device performance. However, higher resistivity and thermal conductivity SiC substrates have proven superior for HEMT power applications. To improve the breakdown voltage and thermal profiles of GaN-on-Si HEMTs, techniques such as localized etching of the Si substrate in the access region or transfer of the III-N epitaxial layers onto alternative substrates such as quartz and diamond have been reported [1-3]. Azize has studied the effect of gradual backside substrate dry plasma etching on the AlGaN/GaN heterostructure [4]. While an increase in 2DEG carrier density (N_{SH}) was reported when the substrate was thinned from 500 to 350 µm, a plastic deformation of the structure occurred when the substrate thickness was further reduced to 150 um, evidenced by cracks in the GaN epi and reduced electrical performance. In this work, we quantify the influence of chemical mechanical polishing on the substrate-induced strain and HEMT performance. We further address the possibility for minimizing performance degradation by post-CMP localized substrate etching.

Four-inch wafers of commercially available $Al_{0.27}Ga_{0.73}N$/GaN HEMT structures grown by metalorganic CVD on 575 µm thick (111) Si substrates were thinned by backside grinding and chemical-mechanical polishing (CMP) to 200 µm and 150 µm. The average sheet resistance (R_{SH}), measured by a non-contact Lehighton instrument over the entire wafer, increased by less than 5% in both cases (Table I). The bow parameters on the 575 µm, 200 µm, and 150 µm thick wafers (wafers A, B, and C) were measured to be concave with values of 41, 220, and 314 µm, respectively (Fig. 1). The Raman frequency of the E_2 phonon line of the GaN buffer, stimulated using a 532 nm green laser, was used to calculate the additional in-plane stress caused by substrate thinning for each wafer [5]. For wafers B and C, the blue shift of the E_2 phonon line indicated additional compressive stress, calculated to be 0.83 and 1.42 GPa, respectively (Fig. 2a). A sample from wafer B (200 µm thick) was subjected to the conditions of the Ohmic contact rapid thermal annealing process (850 °C, 30 sec., N_2). A further increase in both R_{SH} and additional compressive stress were observed (Fig. 2b, Table I). Therefore, substrate thinning and subsequent annealing introduced compressive stress in the substrate, which counteracted the tensile strain in the AlGaN barrier, reducing the piezoelectric polarization and N_{SH}, resulting in increased R_{SH}. It should be noted, however, that substrate thinning by CMP down to 200 µm did not significantly change the AlGaN/GaN surface morphology.

Subsequently, HEMT devices were processed on samples diced from the 200 µm thick wafer. Standard sample handling and fabrication methods were employed: Cl-plasma mesa etching, Ti/Al/Ni/Au Ohmic contacts alloyed by rapid-thermal annealing, Ni/Au gate lift-off, and 100 nm thick PECVD SiN passivation. The DC current-voltage characteristics are presented in Fig. 3. Hall measurements indicated a reduction in N_{SH} by about a factor of 3 to ~$3x10^{12}$ cm^{-3}, consistent with the increase in R_{SH} measured on the RTA-annealed control sample (Table I). However, RTA-induced R_{SH} degradation can be avoided by Ohmic contact deposition prior to substrate thinning.

In order to remove the rest of the Si substrate, a localized Si etch process was developed for vias with target aspect ratio of 20:1 [6]. This process would enable the etch of 10 µm-wide trenches localized underneath the source/drain access region using GaN heterostructures on 200 µm thick Si. Subsequently, such trenches can be selectively lined with high thermal conductivity, stress-engineered NCD films for improved substrate-side near-junction electrothermal management [7, 8].

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Table I. Comparison of AlGaN/GaN HEMTs as a function of substrate thickness and high temperature annealing.

Wafer/sample	Thickness (µm)	R_{SH} (Ω/sq)	ΔR_{SH} (%)	$E_{2,GaN}$ (cm^{-1})	$\Delta\sigma_{xx}$ (GPa)	Bow (µm)
A, as-grown	575	480.6	-	567.03	-	41
B, as-grown	200	501.7	4.3	567.31	0.81	220
B + 850 °C RTA	200	1289	168	567.49	1.33	-
C, as-grown	150	504.2	4.9	567.52	1.42	314

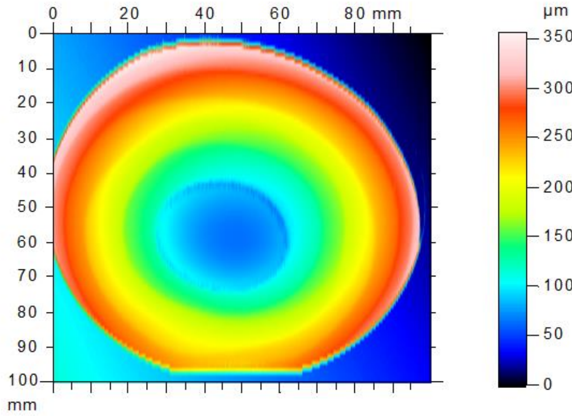

Fig. 1a. Concave bow profile of wafer B (200 µm thick).

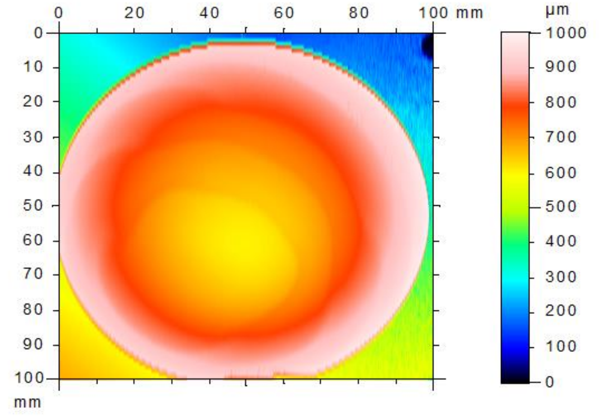

Fig. 1b. Concave bow profile of wafer C (150 µm thick).

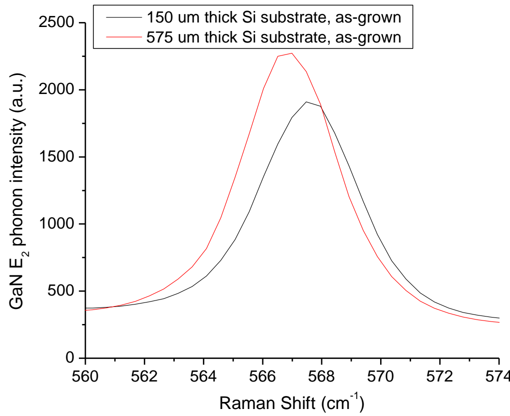

Fig. 2a. Raman E_2 phonon line positions on wafer A (575 µm thick) and C (150 µm thick substrate).

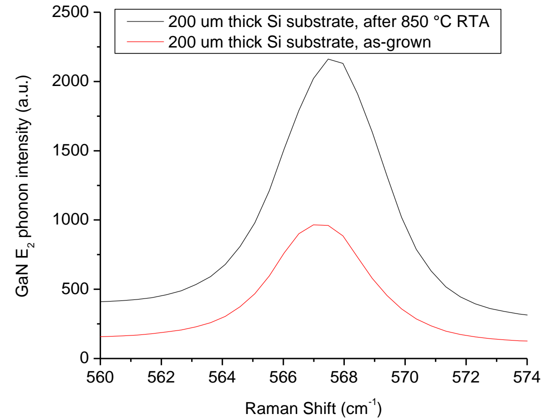

Fig. 2b. Blue-shift effect of an RTA anneal on the Raman E_2 phonon line position on 200 µm thick AlGaN/GaN/Si samples (wafer B).

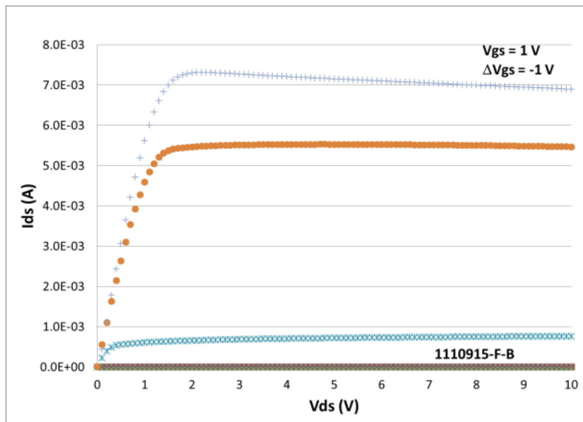

Fig. 3a. I_{DS}-V_{DS} characteristics of HEMTs fabricated on samples from wafer B, CMP-thinned to 200 µm.

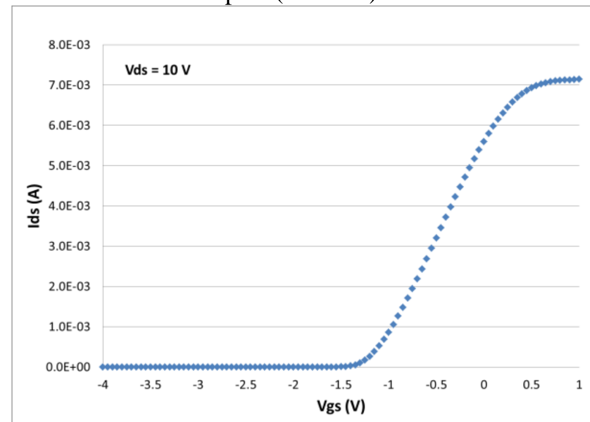

Fig. 3b. I_{DS}-V_{GS} (V_{DS} = 10 V) characteristics of HEMTs fabricated on samples from wafer B (200 µm thick).