Above 2000 V breakdown voltage on 2 µm-thick buffer ultrathin barrier AlN/GaN-on-Silicon transistors

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New emerging high power applications push industrials to develop a new generation of power devices working above 1 kV with high efficiencies. GaN's wide band-gap semiconductor properties and the compatibility with silicon technology lead to high expectations in low-cost power electronics with breakthrough performance, especially for high voltage DC-DC converters. Double Heterojunction field Effect Transistors (DHFET) have already demonstrated high performances combining high breakdown voltage, high sheet charge density and high electron mobility on silicon substrate. However, this technology still suffers from the limitation of the silicon substrate since the breakdown occurs when the electric field reaches the silicon for large gate to drain spacing. In order to overcome this limitation, we have developed a process in which we locally remove the Si substrate in the sensitive area (between gate and drain).

A schematic of the epitaxial structure used for this study as well as a SEM picture of the back-side ring around the drain after the silicon etching are represented in Fig. 1. An AlN/GaN/AlGaN double heterostructure has been grown by metal organic chemical vapor deposition (MOCVD) on a 4 in. Si (111) substrate with a buffer thickness of about 2 µm. A 3.0-nm-thick in situ Si_3N_4 cap layer was deposited on top of the 6.0 nm ultrathin AlN barrier layer. High electron sheet concentration of 2.1×10^{13} cm^{-2} with a mobility of 900 $cm^2.V^{-1}.s^{-1}$ were measured by room-temperature Hall measurements. The process used to fabricate the devices can be found in [1]. It has to be pointed out that no source field plates or gate dielectrics have been implemented in these devices. The Si back side removal has been performed on part of the cells across the wafer so that a proper comparison without growth and/or process variation can be achieved.

DC characteristics of 50 µm width AlN/GaN devices including a gate to drain distance of 30 µm with local Si removal are shown in Fig. 2. Low off-state device leakage current is observed in spite of the high electron density and the ultrathin barrier layer well below 10 nm. Maximum open channel current density is close to 250 mA/mm for this design and is mainly limited by the thermal dissipation after Si removal. As can be seen in Fig. 2, a unique breakdown voltage above 2 kV can be achieved on these devices while maintaining an on-resistance below 3 mΩ cm^2, showing the effectiveness of this approach. The three-terminal breakdown voltage measurements of this transistor design at V_{GS} = -5 V with and without Si local removal are represented in Fig. 3. A huge improvement of the hard breakdown voltage from 700 V to 2.1 kV can be noticed, which is not limited anymore by the Si substrate in these devices using a buffer thickness as low as 2 µm. However, the higher drain leakage current as compared to the gate leakage current clearly shows that the electron confinement can still be improved. Also, multiple field plates are needed to avoid gate degradation under such high electric fields. These improvements may allow the demonstration of 3 kV breakdown voltages in GaN-on-Si devices.
Finally, an AlN thick layer (8 to 10 µm) delivering high breakdown field (> 4 MV/cm) followed by a Cupper metallization will be deposited inside the trenches to significantly improve the thermal dissipation without degrading the outstanding breakdown voltage.

[1] N. Herbecq et al, Applied Physics Express 7, 034103 (2014)

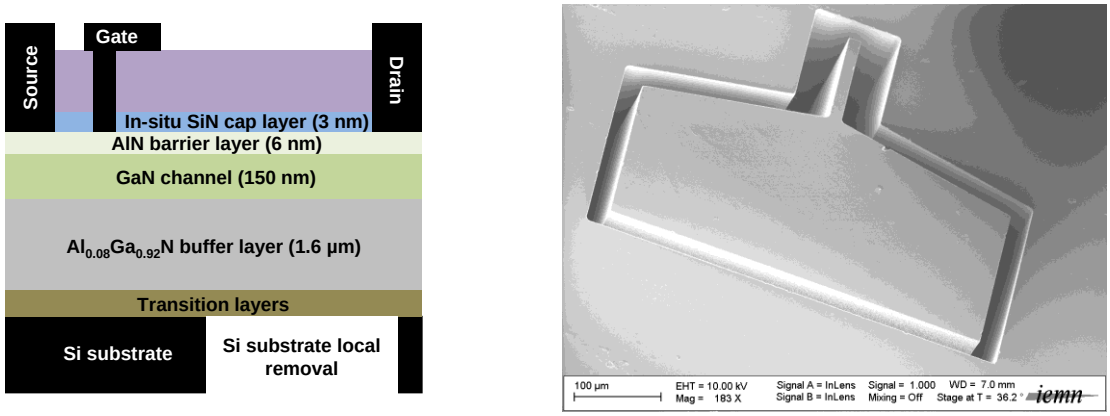

Fig. 1: Schematic cross section of the AIN/GaN/AlGaN DHFET with the local substrate removal and SEM picture of the back-side ring around the drain after the silicon etching

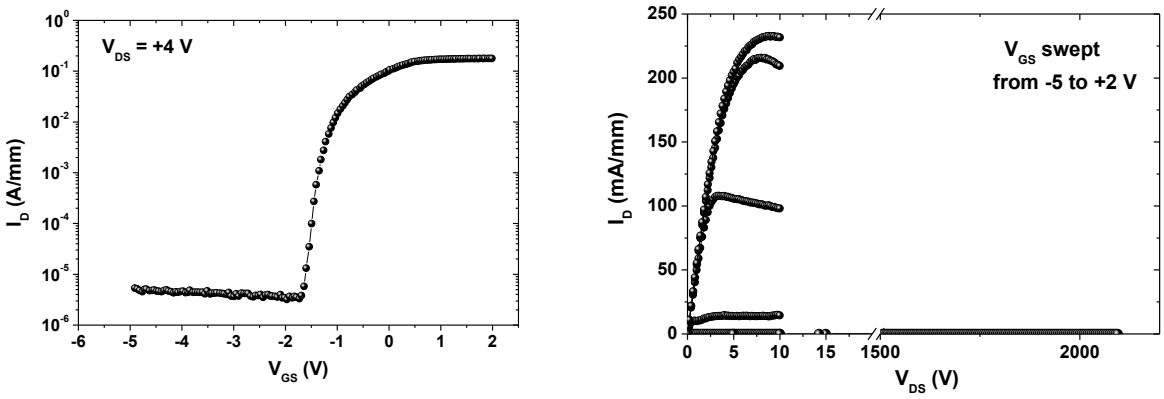

Fig. 2: Transfer characteristic at V_{DS} = 4V (left) and I_D–V_{DS} characteristics (right) of a 1.5×50 µm AlN/GaN-on-Si DHFET with L_{GD} = 30 µm after local substrate removal.

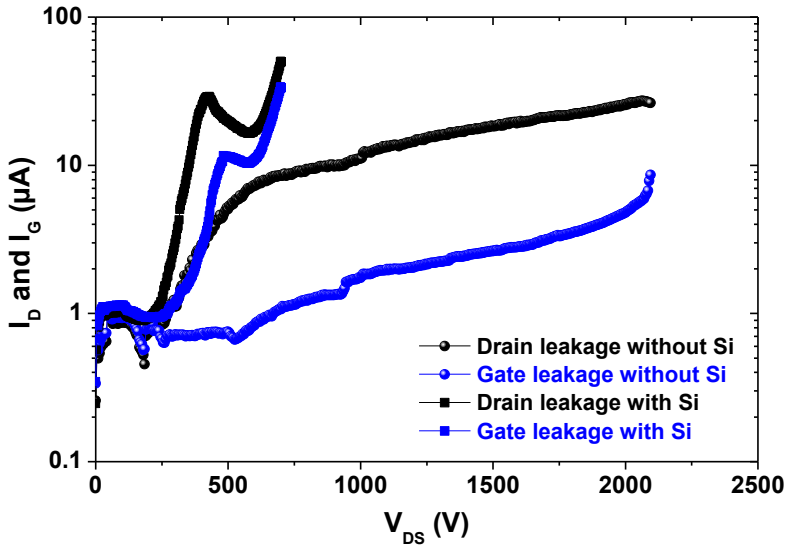

Fig. 3: Off-state characteristics of a 1.5×50 µm AlN/GaN DHFET with L_{GD} = 30 µm before and after local substrate removal at V_{GS} = -5V.

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