Using GaAs Diesort Methods for Efficient High Volume Capacitor Testing

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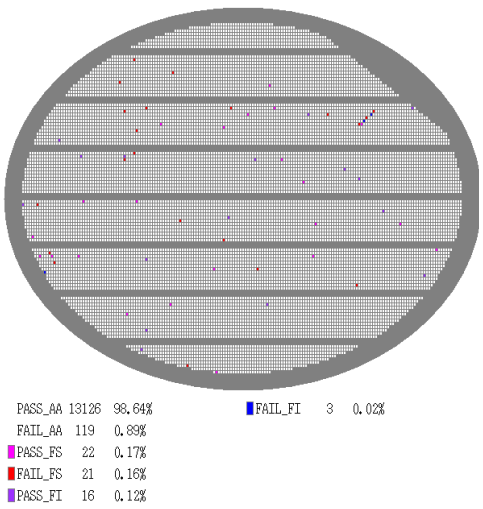
Abstract

Diesort multi-site probe cards and methodologies for GaAs integrated circuit die have been used for multi-faceted characterization of MIM capacitor leakage currents and ramp-to-breakdown voltages for processes under development. By transforming the die inside the bond pads with taps into that circuit's capacitors and using those same bondpads for designed arrays of capacitors, we have been able to do both overvoltage stress and ramp to breakdown testing on almost 100 thousand capacitors per wafer (over 25 cm^2 of total capacitor area) in a short time, enough volume to allow us to characterize accurately capacitor defects at a sub-0.1% level, something impossible with normal capacitor PCM test quantities.

We report on studies of how process variants affect capacitor leakage, overvoltage response, and 4V/sec breakdown voltage and on how this electrical test can be used to assess effectiveness of in-process Automated Visual Inspection for screening out "weak sister" capacitors. Reliability testing was also carried out before and after a variety of stresses and results of that will be reviewed.

Fig. 1



During wafer fab, Automated Visual Inspection (AVI) is done and images are stored. Based on AVI data, each die is assigned a bin of PASS (no defect) or FAIL (at least one capacitor defect).

After the wafer is fully processed, a capacitor leakage test is done. For each capacitor, leakage current is measured four times: first at a low voltage, then at two different stress voltages, and again at low voltage after stress. The total stress time for each capacitor is 1100 ms. To minimize test time, the leakage current for 24 capacitors (3 die sites, 8 capacitors per die site) is measured in parallel. The test time for a wafer with 13307 die sites (> 100K capacitors) is about 2.5 hours.

Fig. 2

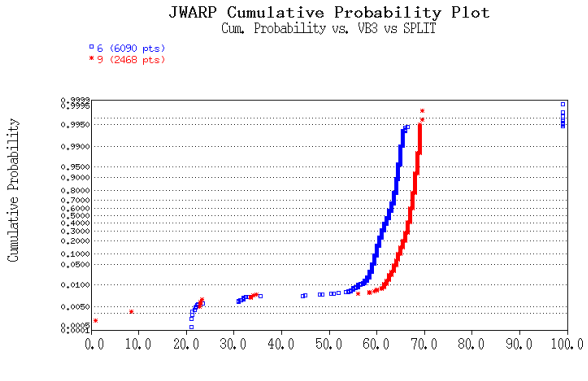


Fig. 1 shows a wafer map of the combined AVI and Capacitor test data obtained with this method. For die with visible defects which failed a capacitor leakage test, the saved AVI images provide the defect location to guide failure analysis.

Capacitor ramp-to-breakdown voltage data can also be collected using this multi-site, parallel test method. The ability to collect large quantities of data in reasonable time is helpful in assessing layout and process variations. For example, Fig. 2 compares the ramp breakdown voltage for wafers with differing MIM Capacitor process parameters.