Effect of Pt thickness on the gate sinking in a pHEMT device

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Abstract

Diffusion of gold from the gate metal contact into the active layer is one of the frequent causes of pHEMT device failures. As the gold from the gate sinks towards the channel an increase of the on resistance is seen along with poor device performance. A titanium layer and a platinum layer is used to prevent this from happening. However, gate sinking can still occur even with this diffusion barrier. In this study device characteristics with varying Pt thicknesses and its effect on overall gate sinking is investigated. It is found that increasing the thickness does not necessarily prevent gate sinking. In fact, more gold diffusion is seen with increasing Pt thickness.

INTRODUCTION

The gate metal sinking in a pHEMT device can severely impact the device performance and reliability [1]. Generally Ti/Pt/Au gate metal stack is used in the GaAs integrated circuit products. The first Ti layer is deposited to ensure good adhesion at the semiconductor surface. Next, the Pt layer is used as a barrier to stop Au diffusion through the bottom Ti layer and into the semiconductor. However, gate metal can still diffuse into the semiconductor. Chou et al. [2] have observed Ti inter-diffusion in a device during high temperature accelerated life test. High gate leakage current is also observed in a delta gate device due to Au diffusion near the edge of the gate metal [3]. In a delta gate structure, Au can deposit on the side walls of the gate stack during metal deposition. This unwanted Au can diffuse into the semiconductor in the subsequent process steps and alter the device characteristics. The deposition of Au on the side walls could be related to the stress of the Pt layer, which increases with the increase of the thickness. In order to minimize the Au deposition on the side walls devices with varying Pt barrier thicknesses are manufactured and studied.

DEVICE PROCESSING AND TESTING

Three groups of pHEMT devices with delta gates (0.5 µm) are manufactured using a standard double recess GaAs integrated circuit process flow. The gate metals are deposited on an InGaP etch stop layer after the gate recess. In the first group of wafers, the Pt thickness is about 200Å. In the second and third groups of wafers, the Pt thicknesses are about 500 and 1000Å respectively. All wafers are processed together before and after the gate metal deposition to keep other processing conditions consistent. All gate metals are deposited using the same CHA evaporation system. After finishing all process steps a Keithly production test stand is used to test the standard 200 µm FETs. To study the gate sinking, one wafer from each group is annealed at 300°C for 10, 20, and 30 minutes. The wafers are then tested after each anneal to record the change of the critical FET parameters.

RESULTS AND DISCUSSION

The pinch off voltages (Vp) for each wafer is measured before any annealing is done to observe any difference between Pt thicknesses before gold diffusion. The Vp values are measured at 2.5% of Idss of the devices and are shown in figure 1. From this figure it can be seen that all the wafers have a median pinch off voltage around -1.1V. This indicates that there is almost no gold diffused into the channel after metal deposition regardless of the Pt thickness.

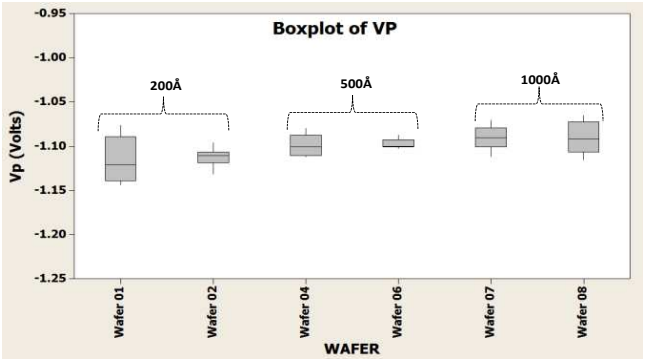

Figure 1: Pinch off voltages (Vp) measured at 2.5% of Idss. The above values are taken before any anneal testing.

To further characterize the effect the varying Pt thicknesses has on the device electrical properties the breakdown voltage (Vb2) and the on resistance are also measured and can be seen in figure 2 and figure 3. The devices with 200 Å of Pt show a slightly higher Vb2 (~ 20 V) measured at 1 mA/mm compared to the other devices. It could be related to slightly lower doping in the Schottky layer. The devices with 500 and 1000 Å of Pt show a similar Vb2 of around 17 - 18V. The on resistances, measured at the drain source linear zone at a gate bias of about 0V, are about 1.25 Ohms-mm for all the devices, which is another indication that the different Pt thicknesses in the gate metal

stack do not change the channel characteristics before annealing [4].

After each anneal, the wafers are tested to record the change of the critical FET parameters. The change in the pinch-off voltage (delta Vp) and the on resistance (delta Ron) is the difference between the prior anneal Vp/Ron values and the post anneal Vp/Ron values. These are calculated after each anneal of 10, 20 and 30 minutes.

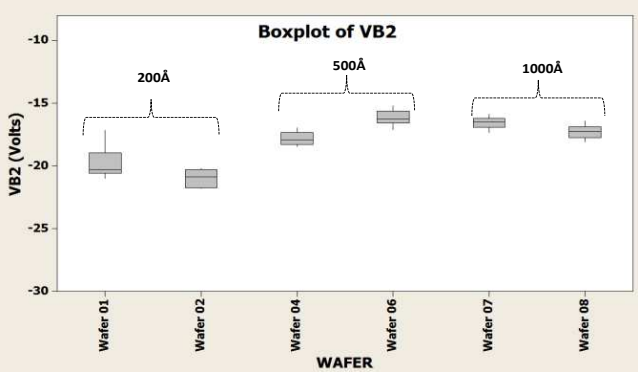

Figure 2: Gate drain breakdown voltages (Vb2) measured at 1mA/mm current before anneal testing.

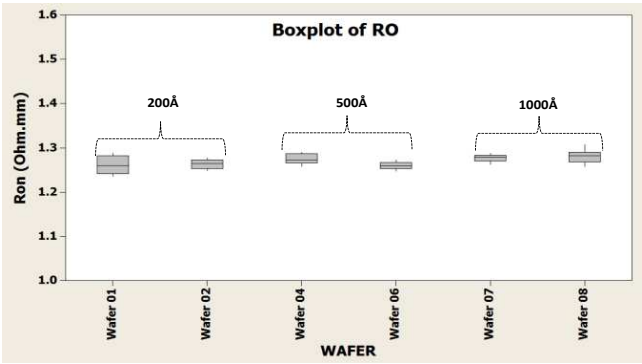

Figure 3: On resistances measured at the drain source linear zone at a gate bias of 0V. Measured before anneal testing.

Figure 4 shows the box plot of delta Vp for the wafers with different Pt thicknesses in the gate metal stack. The positive shift indicates that the Vp decreases (becomes less negative) after each anneal. The Vp for the 1000 Å Pt devices shifts about 45 mV which is much greater compared to the shifts for the 200 and 500 Å Pt devices for 10 minutes of annealing. However, the shifts for 200 and 500 Å of Pt are negligible. As the annealing time increases to 20 and 30 minutes, the values of delta Vp also increase for all of the devices. The largest increase is observed in the devices with 1000Å of Pt.

The box plot for delta Ron and gate drain leakage current measured at -7 V are shown in figure 5 and figure 6. The delta Ron exactly follows the trend of the delta Vp. The bigger shift in Vp and the increase in Ron are most likely due to the diffusion of gold into the semiconductor during each anneal. Therefore, the gate metal (i.e. gold) and the semiconductor interface moves closer to the channel with the increase of annealing time which means the gate requires less voltage to turn off the channel. The increase in Ron is due to more diffusion of gold, which reduces electrically active area of the channel, where the carries encounter more resistance. The diffusion of gold into the semiconductor during thermal annealing is responsible for the increase of the leakage current, which was also observed by J. Oerth et al. [3]. Most likely the deep levels related to gold in the AlGaAs layer generate higher leakage current in the devices.

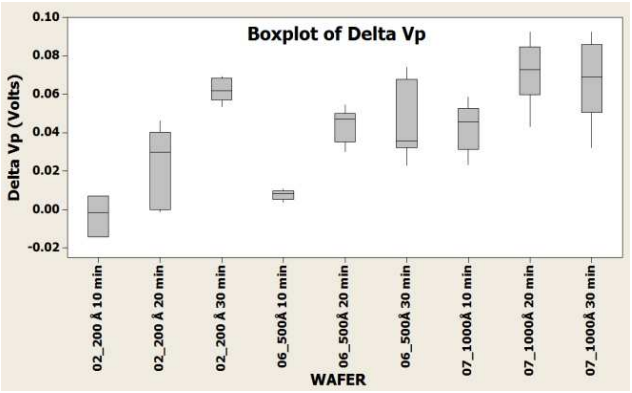

Figure 4: Boxplot of delta Vp for varying Pt thickness after 10, 20 and 30 minutes of annealing at 300°C.

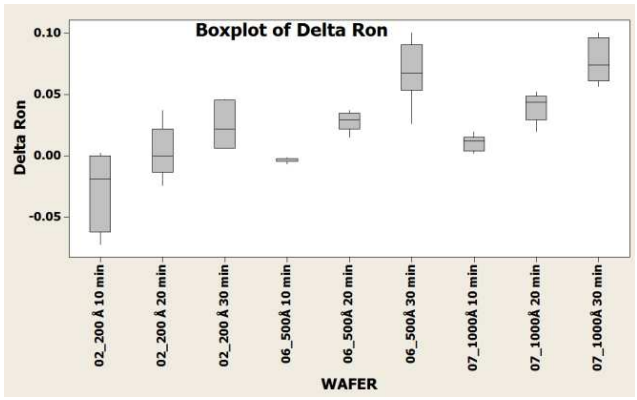

Figure 5: Box plot of delta on resistances for varying platinum thicknesses after each anneal step.

In order to confirm the Pt thickness and gold diffusion in the semiconductor, focus ion beam induced (FIB) scanning electron micrographs are taken from each device. Figure 7 shows the cross-sections of the gates before and after the annealing of the devices. The picture clearly shows the different Pt thicknesses (200, 500 and 1000Å) in the gate metal stack. The diffused gold is also visible at the edge of the gates of the devices after annealing. More gold diffusion is seen in the devices with 1000Å of Pt. This observation agrees very well with the bigger shift of Vp and Ron in the

devices with 1000 Å of Pt. In another investigation EDS mapping was used to confirm the gold diffusion. Furthermore, J. Oerth et al. [3] showed dominant gold diffusion at the end of the gate foot by EDS.

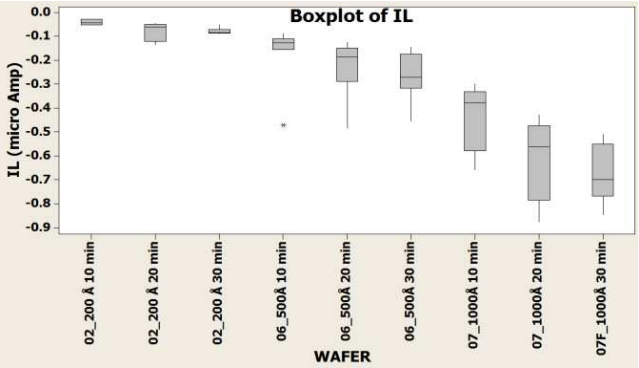

Figure 6: Box plot of the gate drain leakage current measured at -7 V.

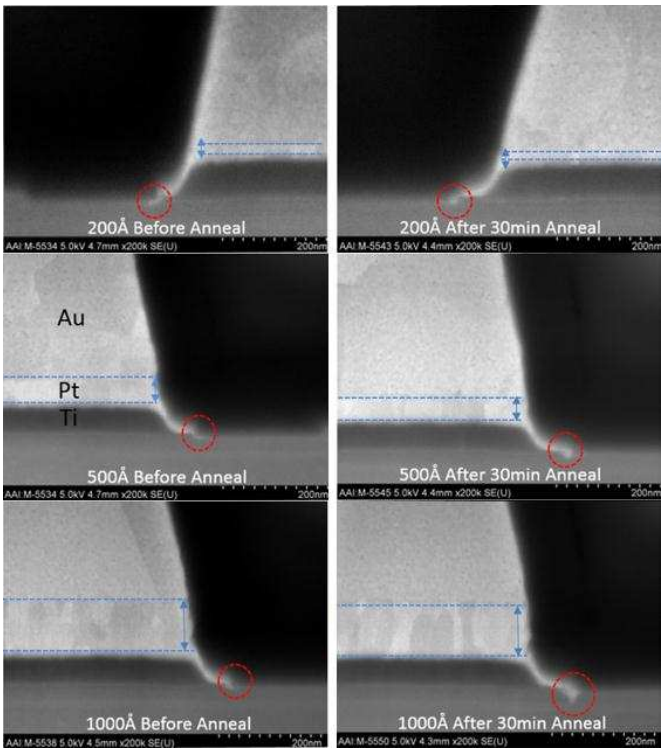

Figure 7: FIB cross-sections of the gates before and after the total anneal time of 30 minutes at 300°C.

The variation of surface stress (stress and thickness product) as a function of film thickness of different elements is reported in MTL Annual Research Report 2013 [5]. It is seen that the surface stress increases significantly with the increase of Pt film thickness. Therefore, the higher shift of all the critical FET parameters in the wafer with 1000Å of Pt could be related to higher stress during Pt deposition, which pulls the resist and increases the aperture of the photoresist opening. The increase in the opening enhances the probability of Au deposition on the side walls of the stack. This also increases the possibility of the Au touching the semiconductor surface which, in turn, can increase the leakage current and contribute to gate sinking (higher shift in Vp and Ron). The lower Pt thickness reduces the possibility of gate sinking due to lower stress during deposition. The stress of a 1000Å Pt film deposited on 50 Å Ti is around 800 MPa (tensile). Thermal loading for the thicker Pt film may not have significant contribution due to longer throw distance.

The gate sinking problem can be reduced by optimizing the photoprocess, metal deposition process and using lower temperature in the subsequent process steps.

CONCLUSIONS

It is found that, before annealing, different Pt thicknesses have little effect on the gold diffusion and hence the electrical performance of pHEMT devices for a Ti/Pt/Au/Ti gate metal stack. However, when the devices are annealed it is seen that there is greater gate sinking in devices with more Pt. Therefore, to prevent Au diffusion from occurring during device testing and operation, a thinner layer of Pt should be used. Using less Pt will cause less stress in the photoresist during deposition which will reduce the chances of the photoresist pulling back to allow Au to deposit on the side walls and then to later diffuse into the channel.

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ACRONYMS

FET: field effect transistor
FIB: focused ion beam
pHEMT: pseudomorphic high hlectron mobility transistor