Development of an InP/GaAsSb DHBT MMIC Process with a Teflon AF Interlevel Dielectric

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Abstract

In the present work we report the development of and first results for a millimeter-wave integrated circuit (MMIC) process based on InP/GaAsSb double heterojunction bipolar transistors (DHBTs) using amorphous fluoropolymer (Teflon AF) as the interlevel dielectric. Teflon AF is used instead of benzocyclobutene (BCB) which degrades device performance due to its high temperature curing cycles. Additionally, Teflon AF exhibits superior dielectric properties with a relative dielectric constant of $\varepsilon_r = 1.9$ and a dissipation factor of 2×10^{-4} at 1 GHz. An inverted microstrip topology was chosen for the passive elements, and first results for transmission lines and amplifiers are shown in this report. To the best of our knowledge, our work is the first demonstration of III-V based millimeter-wave MMICs using a Teflon planarization.

INTRODUCTION

Several groups have presented InP DHBT based MMICs at frequencies up to ~ 600 GHz [1, 2]. To the best of our knowledge, all of these technologies use BCB as the interlevel dielectric even though it has been shown that the necessary BCB curing cycles at temperatures around 250 °C can degrade device performance [3]. Single devices using Teflon AF planarization have been presented and showed no performance degradation when compared to air-bridge devices [4]. The newest generation of such devices is comparable to state-of-the art DHBT technology, exhibiting simultaneous cutoff frequencies of $f_T/f_{MAX} = 503/780$ GHz [5].

A complete MMIC design-kit based on InP/GaAsSb DHBTs using two Teflon AF interlevel dielectric layers has been developed in order to provide a suitable technological platform for future millimeter-wave applications. The design-kit includes DHBTs, MIM-capacitors, resistors, GSG-pads, through-substrate vias, transmission lines and discontinuities such as bends and junctions.

PROCESS DESCRIPTION

In Fig. 1 the schematic representation of the wiring cross-section is shown. The fabrication of the MMICs starts by the formation of the DHBTs [4, 5] up to isolation mesa etching. At this point all the active layers have been etched, except in the active device region, and the bare semi-insulating InP substrate is exposed.

Next, the device contact post metallization (Metal 1) is deposited. It also also serves as landing pad for the vias, bottom electrode of the MIM-capacitors and can be used for dense wiring if necessary. The thin film resistor metal exhibiting a sheet resistance of 25 Ω/□ is deposited onto the substrate. Device planarization is achieved by spinning a Teflon AF layer and subsequently dry-etching it to expose the device contact posts resulting in a Teflon 1 layer thickness of approximately 1 µm. In the next step, openings are etched into the Teflon 1 layer in order to expose the resistor metal, the bottom electrode of the capacitors and the via landing pads. A 60 nm thick SiN layer is then deposited over the whole sample and patterned to form the insulator of the MIM capacitor with approximately 1 fF/µm^2. The 900 nm thick Metal 2 layer is evaporated to serve as signal conductor, contact the DHBTs, the resistors and form the top electrode of the capacitors. The interlevel dielectric is formed by spin coating the sample with an 8 µm thick

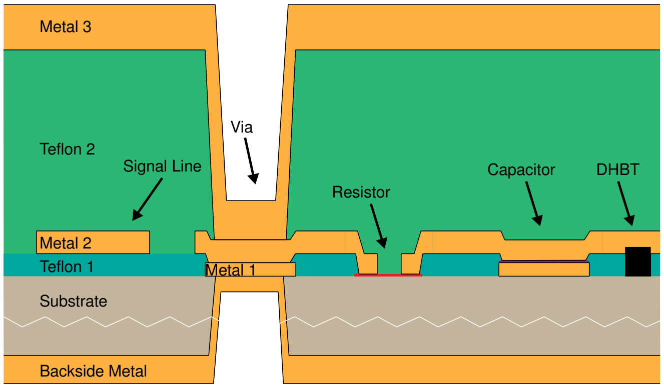

Fig. 1: Schematic representation of the wiring cross-section for the MMIC process developed in this work.

Teflon AF layer (Teflon 2). Vias are etched into the Teflon to access the Metal 2 layer, which is necessary to make the transition from inverted microstrip to co-planar GSG-pads and to ground the substrate to suppress parasitic modes. Finally, Metal 3 is electroplated and completes the inverted microstrip structure with Metal 2 as the signal line and Metal 3 the ground plane.

For high frequency applications additional backside processing is necessary. First, the substrate is thinned down from 350 μm to 50 μm, then through-substrate vias are dry-etched and finally a thick backside metallization is electroplated. The through substrate vias connect the top ground plane (Metal 3) with the backside metallization in order to suppress substrate modes. All results presented in this work were however achieved with the full substrate thickness of 350 μm.

INVERTED MICROSTRIP TRANSMISSION LINES

The inverted microstrip structure provides excellent confinement of the electric field, making the MMIC insensitive to packaging especially in combination with the backside processing. A Teflon 2 layer thickness of 8 μm was chosen so that transmission lines with impedances between 30 Ω and 100 Ω can be fabricated but are narrow enough to allow for dense wiring and small MMIC footprint. A 10 μm wide signal line on the Metal 2 level results in a transmission line with an impedance of approximately $Z_0 = 55\ \Omega$ and and effective relative dielectric constant of $\varepsilon_{r,\mathrm{eff}} = 3.8$.

Transmission lines with a length of ~2 mm were characterized up to 220 GHz and the losses are shown in Figure 2. The measured loss is 0.9 dB/mm at 110 GHz and 1.6 dB/mm at 220 GHz, and shows a linear behavior over the complete frequency range. This indicates that for a transmission line without discontinuities, no parasitic modes are excited up to 220 GHz even with the full substrate thickness. However, if bends, junctions or other discontinuities are introduced, this is no longer true and losses significantly increase above 110 GHz making the backside processing necessary for MMICs operating above W-band.

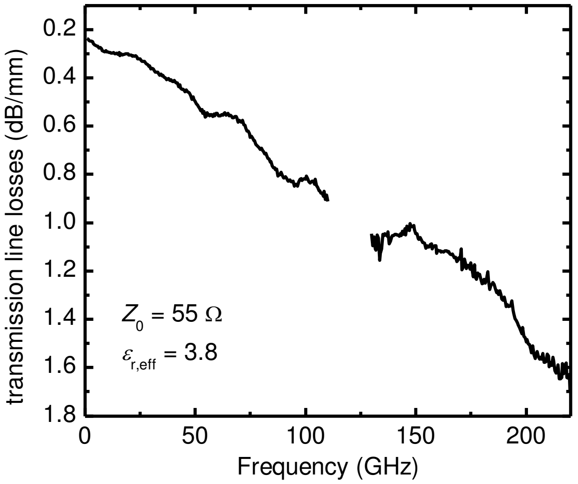

Fig. 2. Measured loss for a 10 μm wide inverted microstrip transmission line up to 220 GHz. The impedance of the line is 55 Ω and $\varepsilon_{r,\mathrm{eff}} = 3.8$.

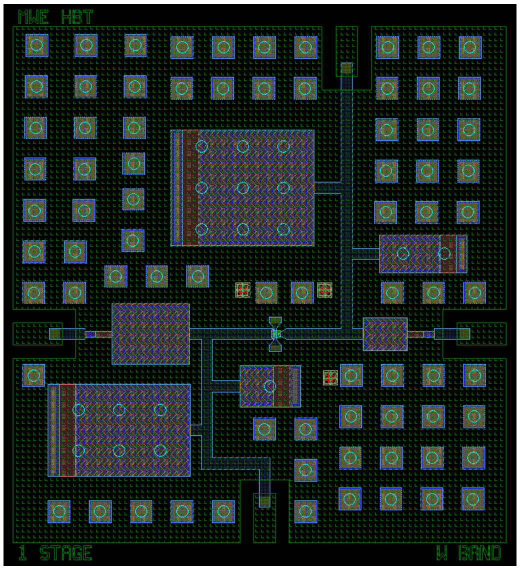

Fig. 3. Mask layout of a one-stage W-band amplifier consisting of a single common-emitter DHBT. The RF-input is on the left and RF-output is on the right. DC supply pads are at the top and bottom of the circuit.

MONOLITHIC MICROWAVE INTEGRATED CIRCUITS

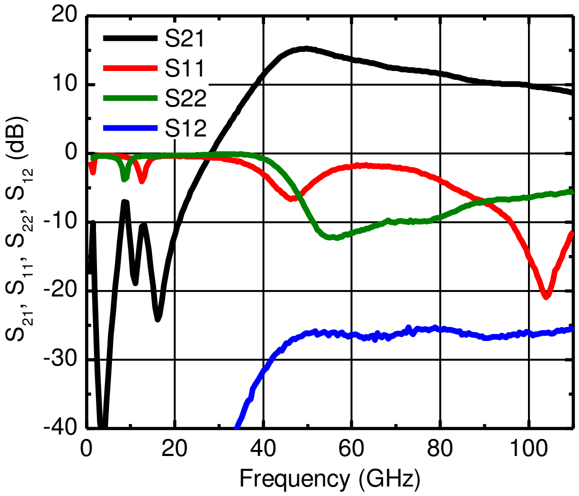

Fig. 4. Measured S-parameters of a one-stage W-band amplifier. The gain is 15 dB at 50 GHz and drops to 9 dB at 110 GHz. Isolation is better than –25 dB over the whole frequency range.

The first batch of circuits intended as a proof of concept includes 1- and 2-stage amplifiers at W- and G-band as well as oscillators at various frequencies from 50 GHz to 200 GHz. Because the backside processing was not yet performed at the time of writing, results above the W-band are not yet available. Therefore, we present a simple one-stage W-band amplifier and an oscillator at 50 GHz. For all the circuits designed in this iteration the same device type was used. The emitter area of $0.3 \times 9.4\ \mu m^2$ is large for high frequency InP based DHBTs in order to achieve high output power while still maintaining excellent RF-performance. Single devices fabricated on the same chip as the circuits exhibit simultaneous $f_T/f_{MAX} \approx 450/600$ GHz at $V_{CE} = 1.2$ V and $I_C = 24.6$ mA.

The W-band amplifier consists of a single common-emitter DHBT, matching circuit and de-coupled DC-feed and RF lines. The mask layout is shown in Fig. 3 with Metal 2 in blue and Metal 3 in green. The RF input and output as well as the DC connections are implemented with coplanar GSG-pads. The RF path leads from the input on the left to the output on the right and is kept straight to minimize discontinuities. Immediately after/before the RF input/output a MIM capacitor is inserted for DC blocking and input/output matching. The DC signal is fed to the device from the bottom for the base and from the top for the collector. The emitter is grounded by two vias to the Metal 3 ground plane. Two capacitors to ground are added to each DC path as RF-short and for matching. The empty space around the circuit is filled with vias in order to ground the substrate and reduce parasitic modes. Circuit simulations of the one-stage W-band amplifier exhibit 12 dB of gain from 70 GHz to 110 GHz with input and output matching better than –6 dB over that frequency range. In Fig. 4 the measured S-parameters are plotted showing gain of 15 dB at 50 GHz which then drops to 9 dB at 110 GHz. Output matching is better than –5 dB over the whole frequency range, while input matching is worse than expected between 70 GHz and 90 GHz. Isolation is better than –25 dB as expected from simulation.

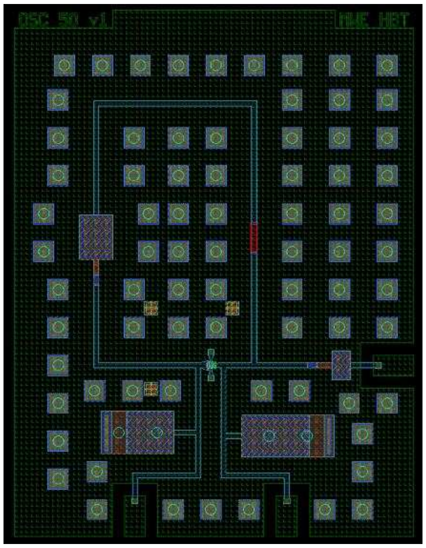

Fig. 5. Mask layout of an oscillator at 50 GHz with a feedback loop from the collector to the base of the common-emitter DHBT. The RF-output is on the right and the DC feeds at the bottom.

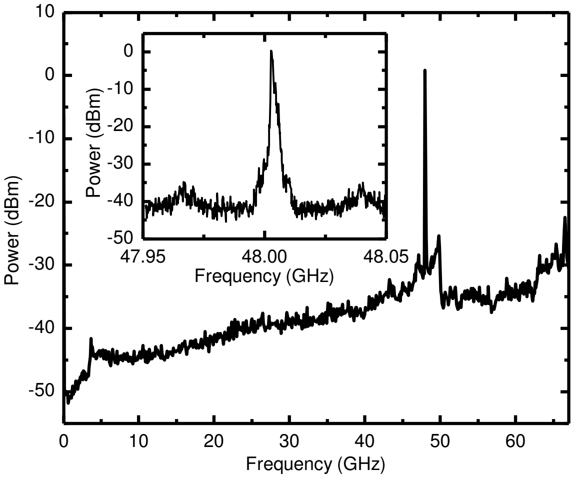

Fig. 6. Measured power spectrum of an oscillator from DC to 67 GHZ showing an oscillation peak at 48 GHz. Inset: Measured spectrum around the peak at 48 GHz.

For the 50 GHz oscillator a common emitter DHBT is biased through two DC-feed lines with capacitors to ground as RF-shorts as shown in Fig. 5. A feedback loop from the collector to the base with a resistor and capacitor in series is used to induce oscillation. On the collector the signal is split between the feedback loop and the RF-output by a T-junction. A capacitor in front of the RF-output pad is used for matching and DC-blocking. The design frequency of the oscillator mostly depends on the electrical length of the feedback path and the value of the capacitance in the feedback loop. The frequency spectrum from DC to 67 GHz was measured and shows oscillation between 47.5 GHz and 51.5 GHz depending on the biasing conditions. In Fig. 6 a spectrum with an oscillation frequency of 48 GHz is plotted. The phase noise is estimated to be –100 dBc/Hz at a 10 MHz offset. Power measurements were carried out with a broadband power meter. The maximum output power for this oscillator is ~1.75 dBm uncorrected, resulting in ~8.25 dBm when taking the probe and cable losses into account.

CONCLUSIONS

We have developed a complete MMIC process including a design-kit based on InP/GaAsSb DHBTs with Teflon AF as interlevel dielectric. The results of transmission lines, a W-band amplifier and a 50 GHz oscillator presented in this work prove the process to work and the technology to be suitable for designing and fabricating MMICs. Multiple reasons for the differences between the simulated and measured results have been identified, the design-kit models updated and the next generation of circuits is currently under development. These circuits are expected to show improved agreement with simulations and superior performance than the ones presented here. In the future more complex circuits at higher frequencies and with more transistors will have to be designed and fabricated to demonstrate the accuracy of the design-kit and the manufacturability of the process. For applications at frequencies ranging from 300 to 600 GHz a more aggressively scaled and optimized device with an f_{MAX} on the order of 800 GHz should be used [5].

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ACRONYMS

BCB: Benzocyclobutene
f_{MAX}: Maximum oscillation frequency
f_T: Unity current gain cutoff frequency
HBT: Heterojunction bipolar transistor
GSG: Ground-signal-ground
MIM: Metal-insulator-metal