Vertical Power Semiconductor Devices Based on Bulk GaN Substrates

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Abstract

In this extended abstract we discuss vertical power electronic device architectures using low defect density (10^4 to 10^6 cm^{-2}) bulk GaN substrates as the starting material and present recent advances. The avalanche capability and ruggedness of the 0.7mm^2 p-n junction diode are supported by test results demonstrating the diode clamping of a 100µH (8mH) inductive load with an initial current of 10 (1.5)A. Double pulse reverse recovery testing results indicate that the reverse recovery time of the vertical GaN PN diode is not discernible because it is limited by capacitance rather than minority carrier storage, and due to this its switching performance exceeds that of the highest speed silicon diode and SiC diode. GaN p-n junction devices with near ideal turn-on characteristics fabricated on rapid ammonothermal grown substrates are also presented. Finally, substrate reliability and cost issues are addressed and a methodology to identify defective devices is discussed.

INTRODUCTION

As the silicon power devices are incrementally improved towards theoretical material property based power device figure-of-merit (FOM) limits, the interest in developing switching power devices based on wide bandgap materials, such as silicon carbide (SiC) and gallium nitride (GaN) has been increasing as these materials have material properties that result in FOM significantly better than that of Si [1-6].

To date, despite the significant development efforts that have been directed toward lateral devices, such as high-electron mobility transistors (HEMTs) fabricated in thin layers of GaN that are grown on foreign substrates, it has not been possible to demonstrate devices that are free of issues that prevent wide-scale commercialization and use. Some well-known issues include reliability failures, dynamic on-resistance, and inability to support avalanche breakdown [6]. By fabricating power semiconductor devices on bulk GaN substrates, it is expected to be possible to realize the material limit potential of GaN including true avalanche breakdown capability and to create vertical architectures that do not suffer from reliability or stability issues associated with thin film surfaces.

In our previous work we have demonstrated various device structures such as p-n diodes and field effect transistors covering breakdown voltages of 600-4000V and forward currents reaching 400A [7-10]. In this extended abstract we advance the state of the art by demonstrating avalanche capability and ruggedness, capacitance dominated reverse recovery, near ideal forward turn-on characteristics and a methodology to improve the yield and reliability of devices fabricated on GaN substrates.

RESULTS

Breakdown characteristics of a p-n junction diode can be observed using a curve tracer as shown in Fig. 1. The curve tracer test provides visual information about the leakage before the onset of the breakdown. Normally a sharp breakdown is desired as this limits the leakage losses and is usually associated with better long term reliability of the device. However, a curve tracer relies on a load resistor to limit the power dissipated on the device thus limits the breakdown current that can be passed in breakdown. Uniform avalanche breakdown across a large area diode can be best demonstrated by testing the device in an inductive load switching test circuit which induces breakdown in the device under test but limits the energy that is dissipated in to the pulse energy. This information is complementary to the breakdown test on a curve tracer in the sense that while large breakdown currents can be forced through the device there is no information about the behavior of the device before the onset of the breakdown. Fig. 2 shows the oscilloscope screen-shot for a GaN p-n diode (0.7mm^2) clamping an 8 mH inductor charged to 1.5 A. The test of the device after the clamping test indicated that the device was still operational. From the waveforms presented in Fig. 2 it can be estimated that approximately 12 mJ was dissipated in the avalanching device without inducing permanent breakdown. Further tests with larger pulse energies are in progress.

The reverse recovery charge of a p-n junction diode impacts the energy losses and maximum switching frequency in the application circuits. The diode turn-off characteristics, measured with a double-pulse test board, for the GaN p-n diode and a SiC diode are presented in Fig. 3. From the C-V characteristics shown in Fig. 4, it can be seen that a capacitive charge contribution of 12 nC is expected during

reverse recovery. Hence, by considering the likely presence of on-board parasitic capacitance it can be judged that almost all of the reverse recovery charge is capacitive. At the same time the comparison with the SiC device of similar ON resistance reveals the superior reverse recovery capabilities of GaN diodes.

While HVPE GaN substrates represent a considerable improvement over heteroepitaxial GaN, they have a number of limitations that have restricted their usefulness for power switches, including diameter, cost, and undesirably-high dislocation density. Recently, Soraa, Inc. introduced a modified ammonothermal approach, known as SCoRA (Scalable Compact Rapid Ammonothermal) that enables high rate growth of low defect density bulk GaN crystals. The SCoRA method, utilizes internal heating rather than external heating as in conventional ammonothermal reactors. Raw material, including seed crystals, polycrystalline GaN nutrient, a mineralizer, and ammonia, are placed inside a capsule and sealed. The capsule is surrounded successively by a heater, a ceramic shell providing structural support and thermal insulation, and an externally-cooled steel outer shell that provides mechanical confinement. The SCoRA reactor has demonstrated capability for temperatures and pressures as high as 750 °C and 600 MPa, respectively, enabling higher growth rates than conventional ammonothermal techniques, but is less expensive and more scalable than conventional autoclaves fabricated from nickel-based superalloys. Consequently, large reductions in the cost of bulk GaN substrates are expected. A conductive SCoRA GaN boule was grown on a free-standing SCoRA GaN seed crystal, as described elsewhere [11]. The boule was then diced into 13mm×13mm squares and ground, polished, and chemically-mechanically polished into epi-ready wafers as shown in Fig. 5. The morphology of the surface as observed by phase-interference microscopy after growth of 15μm of epitaxial GaN on SCoRA substrates is also shown on Fig. 5. The measured p-n diode forward current-voltage characteristics for a 0.11 mm^2 device are shown in Fig. 6 on a logarithmic scale. It is observed that the ideality factor of the diode is n=2 for 8 orders of magnitude in forward diode current. From these curves a hole minority carrier lifetime of 1ns is estimated. A detailed study elaborating the extraction of device model parameters will be published in the future. The breakdown voltage for this device was limited to about 680V as the device was terminated with a simple isolation implant.

Fig. 7 is a summary of Avogy GaN p-n junction diodes and transistors optimized for targeted breakdown voltages covering 1200V to 3.7kV.

Diodes grown on substrates with improper orientation exhibit surface morphology that affects leakage current and reliability. Some examples showing the range of surface morphology across a wafer is shown in Fig. 8. Diodes fabricated from material whose surface is decorated with pyramidal hillocks exhibit excessive reverse leakage current. Typically this abnormal leakage does not arise until a reverse bias of several hundred volts is applied; and infrared luminescence imaging reveals that the leakage path is through the hillock. Not surprisingly, reliability also suffers in this situation. Therefore it is important to minimize the hillock formation through proper choice of substrate orientation; and to screen devices which contain a hillock within their area. Accordingly, as these morphology features are easily visible with white-light interference phase-contrast (Nomarski) microscopy, we have developed a method to evaluate leakage-yield of bulk-GaN-based pn diodes. This technique employs a ZygoTM optical surface profiler to map the surface morphology of an entire wafer; along with an algorithm to predict the fraction of devices which will exhibit high reverse leakage current. The prediction algorithm is based on the height of the morphology features. This is a parameter which is correlated with the reverse leakage current; and particularly the onset voltage at which the excessive leakage appears. Based on this connection between surface morphology and reverse leakage, applied to the morphology mapping, we are thus able to accurately predict the leakage yield of p-n diodes, and to screen devices which would exhibit high leakage. Below we describe the methodology and the prediction algorithm:

Completely map a 2" GaN wafer using a Veeco brand Wyko interferometer after epitaxial deposition and initial patterning. The scan pattern maps the entire wafer with a 1.3% overlap in x and y directions. The data is composited into a single image after a biaxial linear gradient fit to remove any macroscopic tilt in the sample.

The device active area was used as coordinate system and the epitaxial layer was tested at each device location using the initially patterned coordinate system. At each device location 4 failure criteria were applied.

1. Bad pixels – If a threshold number of the data points were registered as NaN the device was considered failed.
2. High Limit – If the maximum height of any pixel was above a threshold value the entire device was considered failed.
3. Low Limit - If the minimum height of any pixel was above a threshold value the entire device was considered failed.
4. Peak-to-Valley Failure: A test (described below) for the local range of heights was applied and if a threshold number of pixels exceeded the threshold the device was considered failed.

For the peak-to-valley algorithm: For each pixel the maximum in a local area, a matrix in the range of 7x7 was tested as was the local minimum and the range was given by Maximum-Minimum. For each device if the number pixels exceeding the threshold were greater than 5% then the device was considered failed.

Fig. 9 shows an example of the application of the above algorithm. By tuning the parameters in the algorithm above, we have been able to predict the wafer sort yield and

reliability that will be obtained from a wafer. Thus, the above algorithm can be used as a wafer selection criterion.

CONCLUSIONS

In conclusion, vertical power electronic device architectures using low defect density (10^4 to 10^6 cm^{-2}) bulk GaN substrates as the starting material were presented. The avalanche capability and ruggedness of the p-n junction diode are demonstrated by test results demonstrating the diode clamping an inductive load with an initial current of 10A. Double pulse reverse recovery testing results indicate that the reverse recovery time of the vertical GaN PN diode is not discernible. Because in the GaN p-n diode there is no minority carrier storage its switching performance exceeds that of the highest speed silicon diode. P-N junction devices with near ideal turn-on characteristics fabricated on rapid ammonothermal grown substrates were demonstrated. Finally, substrate reliability and cost issues are addressed and a methodology to identify defective devices is discussed.

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Figure 1: Curve tracer picture showing breakdown on a GaN p-n diode. The horizontal axis is 200V/division.

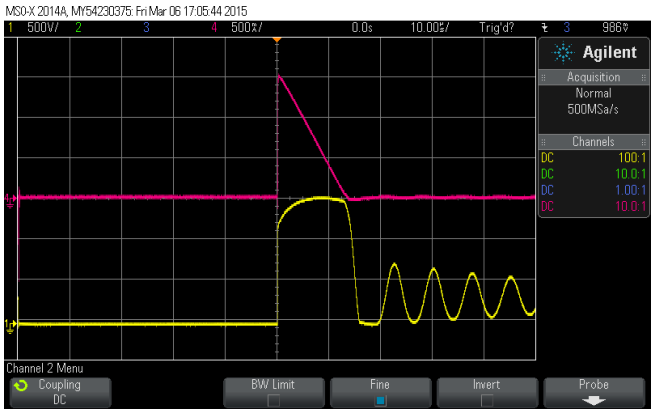

Figure 2: Scope traces showing the diode current (pink) and DUT voltage (yellow), for inductive load testing of a 0.7 mm^2 GaN p-n diode.

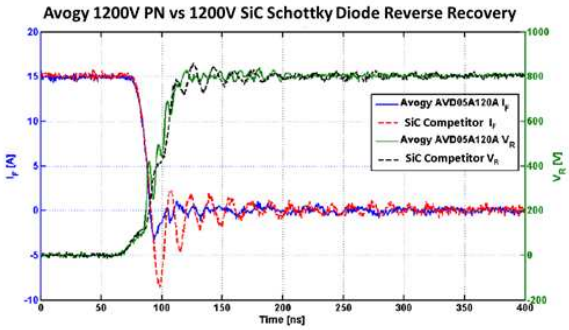

Figure 3: Switching characteristics of a 0.7 mm^2 GaN p-n diode compared with that of a SiC rectifier.

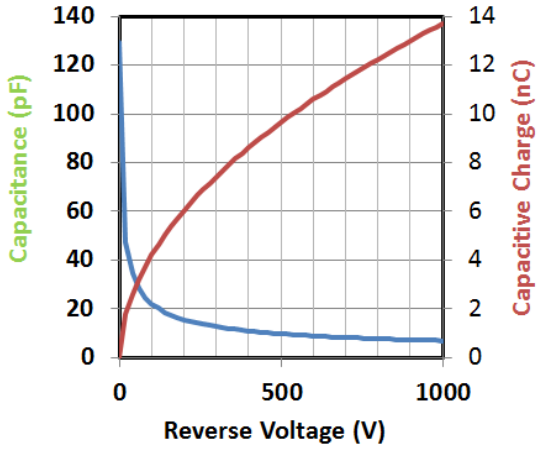

Figure 4: C-V characteristics and integrated charge on a GaN p-n diode with 0.7 mm^2 area.

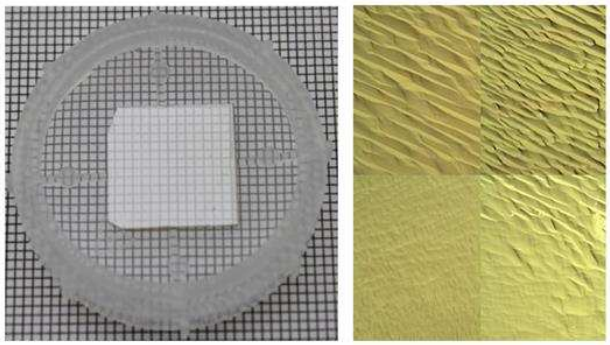

Figure 5: ScoRa substrate ready for epitaxy. Background grid is 1 mm. The right hand side pictures show range of morphology of epitaxial GaN grown on ScoRa wafers.

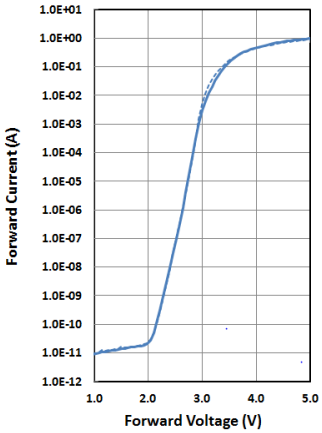

Figure 6: Forward I-V characteristics of GaN p-n diodes fabricated on ScoRa wafers.

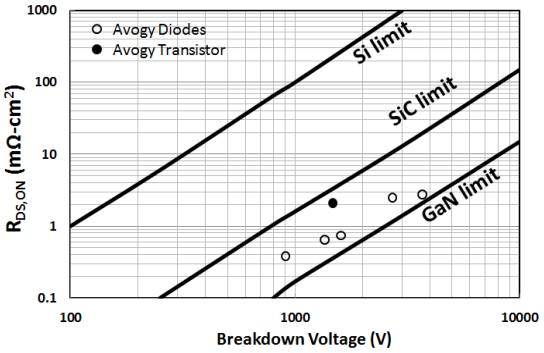

Figure 7: FOM of GaN p-n diodes fabricated by Avogy.

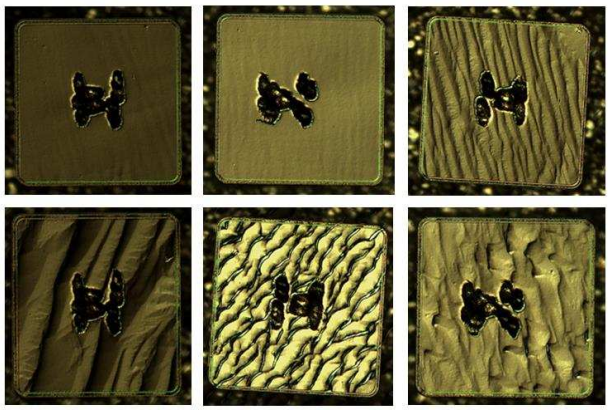

Figure 8: Range of morphological features observed on GaN epitaxy on HVPE GaN substrates. The Nomarski images show anode of p-n diodes. The square is the 4µm thick anode pad. The probe marks on the pads are seen in the middle of the pads.

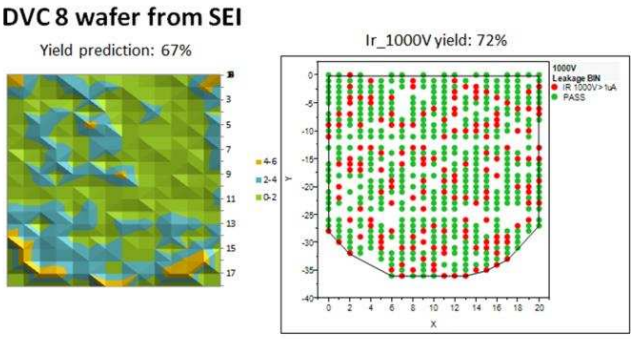

Figure 9: Yield prediction map of the HVPE wafer created by the methodology described in the text (left) and the actual wafer sort yield map of the same wafer after fabrication of p-n diodes (right).