R_{DSON} Stability of GaN High Voltage Power Devices Post Long-Term Stress: A New Method to Screen Unstable R_{DSON} Performers

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Abstract

An innovative method to filter out potentially unstable and unreliable R_{DSON} drifting wafers is demonstrated in GaN-based power devices. Its concept is described and the correlation between screening test and long-term reliability data in terms of R_{DSON} stability is also presented. In addition, we verify that this screening method can predict continuous dynamic R_{DSON} characteristics, which is directly related to application performance.

INTRODUCTION

Adoption of GaN-based heterostructures on Si substrates has been intensively considered in power electronics to achieve higher conversion efficiency and higher system cost competiveness. This is because of the superior material properties such as high breakdown voltage, high carrier density, and high electron mobility, and remarkable technical advances of epitaxial growth on Si. However, for high voltage GaN technology to penetrate the real market, it should demonstrate not only long-term reliability and robustness but also long-term parametric stability. One should also note that there is no industry standard for long-term reliability tests to evaluate GaN-based power devices and predict actual life time from accelerated testing methodologies. In addition, conventional parametric tests have been used to screen out malfunctioned devices in the fab as typically performed in Si technology, but this methodology has failed to identify and predict long-term instability of high-voltage GaN-on-Si heterostructure field effect transistors (HFETs). Especially, on-resistance drift or drain current depression after long-term stress under high-voltage off-state has been one of the well-known issues to be solved in high voltage GaN-based power devices.

In general, it has been considered that R_{DSON} drift is mainly due to electron trapping in GaN-based DC/RF power devices. Extensive attempts to identify physical origin of the trap sites have been made in different groups based on temperature-dependent and field-dependent characterization [1-4]. Typically, carbon-associated traps or other defect-related traps have been reported as a major source of electron trapping in high-voltage GaN-on-Si FETs. However, it is difficult to directly identify its real physical source and implement a solution. Thus, in parallel to making continuous efforts to find the origin of trap sites, it is necessary to develop an early detection technique for high R_{DSON} drifting wafers based on wafer-level characterization without any time-consuming and cost-ineffective long-term test. Figure 1 shows that R_{DSON} drift post 24hr-hot temperature reverse bias (HTRB) stress can predict high R_{DSON} shifter after further stress. This result led us to further investigation about shorter-time stress but the detection efficiency on high R_{DSON} shifter degrades as stress time decreases. Therefore, a way to accelerate R_{DSON} increase has to be developed to improve signal-to-noise ratio for shorter-time stress.

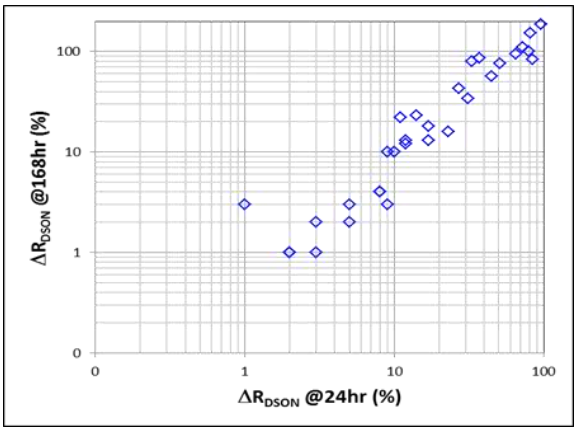

Figure 1 Comparison in R_{DSON} drift between 24hr-HTRB and 168hr-HTRB showing a good correlation in both cases. Note that stress voltage and temperature are 480V and 150C, respectively. $\Delta R_{DSON} = (R_{DSON\ POST\text{-}STRESS} - R_{DSON\ PRE\text{-}STRESS})/R_{DSON\ PRE\text{-}STRESS}$.

In this work, we demonstrate our novel methodology to filter out potentially unstable and unreliable HV GaN HFETs in terms of R_{DSON}. In addition, we will present new reliability tests such comprehensive dynamic R_{DSON} characterization under both voltage and temperature stress, which can provide a more practical reliability performance in actual application.

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SCREENING METHODOLOGY

In order to develop a screening method for R_{DSON} drift due to electron trapping, it is necessary to understand the nature of trapping and de-trapping. The capture and emission via trap sites are a function of electric field, temperature, and time. In principle, for electrons to be trapped under a certain electrical stress, the following three conditions have to be satisfied: 1) empty trap sites are available at one side, 2) electrons to be trapped are available at the other side, & 3) an electric field should be high enough for electrons to be injected from one side to the other. Thus, both stress voltage and stress temperature affects the capture rate of electrons as well as the emission rate of trapped electrons under electrical stress. The competition between the capture rate and emission rate would determine the amount of R_{DSON} drift. And trapping and detrapping processes are also time-dependent because it takes some time for carriers to be emitted or captured when an applied bias switches from off-state to on-state or from on-state to off-state. Both processes continue to progress until the trap sites, actively responding to the current bias condition, are fully occupied or empty.

In general, potential trap sites in AlGaN/GaN based heterostructure on Si substrate are available everywhere since a high density of defects is widely distributed across the GaN-based material grown on the foreign substrate. Thus, it is important to understand how the stress bias would affect entirely GaN-based FETs to better interpret R_{DSON} drift due to trapping effects. In the past years, we have electrically identified the primary source of the R_{DSON} drift from different tests. It has been observed that the epi-layers grown on Si substrates are the major contributor as many other publications have also reported [2, 5].

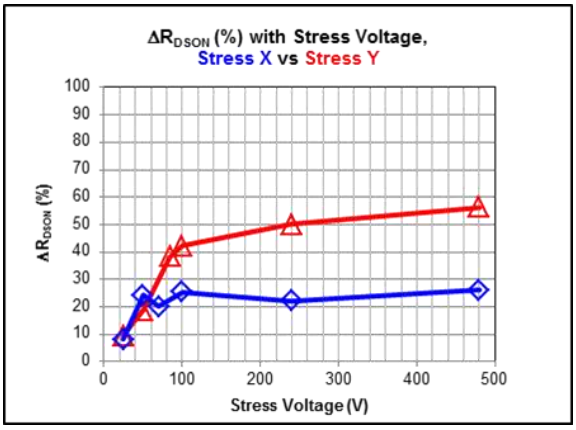

Figure 2 R_{DSON} drift with stress voltage under two different stress types. Stress X (diamond) is a typical off-state stress at V_G = -20V, V_S = $V_{Substrate}$ = 0V, and V_D = 25V to 480V. Stress Y (triangle) is based on a vertical stress.

Figure 2 shows R_{DSON} drift behavior with stress voltage for two different stress types. Stress X is the same as typical reverse bias (RB) stress with the Si substrate grounded. Stress Y is a vertical stress under which the Si substrate is negatively biased while the Source, Gate, and Drain contacts are tied together to the ground. Note that Stress X includes a lateral stress between the Gate and Drain as well as a vertical stress between the Drain and Si substrate while Stress Y has a vertical stress only across the buffer layer. It can be considered that electron trapping under Stress Y would happen preferentially across the buffer layer. Interestingly, both stress cases shows the same trend where R_{DSON} drift increases with stress voltage up to ~100V and then becomes saturated or slowly increases. This indicates that both stress cases can have the same active traps and these traps are across the buffer or epi-layers. Stress Y also gives a much stronger signal than Stress X because the vertical stress includes the buffer beneath the source and gate regions. That is why our proposed pre-screen method is based on the vertical stress.

EVALUATION OF NEW SCREENING METHOD

Figure 3 shows an excellent correlation between our new prescreen methodology (Test A) and long-term R_{DSON} drifting behavior. A low R_{DSON} drifting wafer identified by Test A at high temperature still exhibited a low drift up to 168hr-stress while a high R_{DSON} shifter increased. It clearly demonstrates that a vertical-stress-based Test A can identify high R_{DSON} drifting wafers after long-term HTRB stress. To date, Test A has screened many wafers as low-R_{DSON} shifters. All the low-R_{DSON} drifting wafers have showed a low R_{DSON} drift even after a 1000hr-HTRB stress.

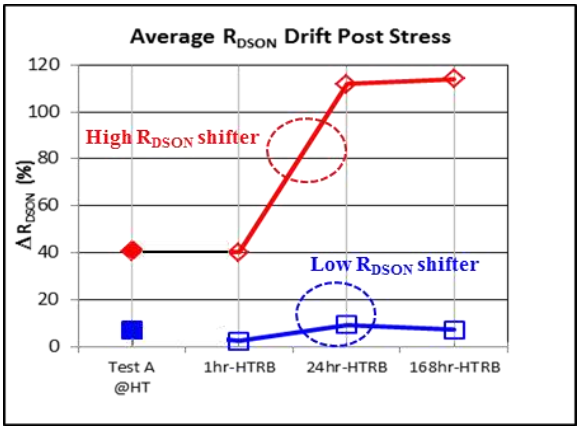

Figure 3 Variation of R_{DSON} drift after two pre-tests (TEST A and B) as well as with HTRB Stress time. Initially, various parts were characterized with Test A & B as new screening methods and were identified as "Low R_{DSON} shifter (Blue Open Square)" and "High R_{DSON} Shifter (Red Closed Diamond)" after long-term stress.

Figure 4 shows the screen results gauged by Test A and continuous dynamic R_{DSON} characteristics of both good and bad groups in R_{DOSN} drift. DC R_{DSON} was first measured at room temperature as a reference. Then, dynamic RDSON measurements were performed at 1 µs-on-state pulse after 10msec off-state stress at a different stress voltage. At each

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stress voltage, both off-state and on-state pulses were switching continuously for 1 minute. Note that the stress biases have been kept on during the dynamic RDSON measurements at 100V to 480V and room temperature. The stress bias of 480V was also kept on while the test temperature increased to 75 ºC and 150 ºC. As shown in Figure 4(b), dynamic R_{DSON} drift behavior became pronounced at high temperatures, attributed to more electron trapping and heating effects. High R_{DSON} shifter by Test A clearly showed high dynamic R_{DSON} drift and even the drift at 150 ºC and 480V-stress gradually increased, indicating that it could be potentially unstable in the application point-of-view. However, low R_{DSON} shifter exhibited much low dynamic R_{DSON} drift and stable at 150ºC and 480V-stress.

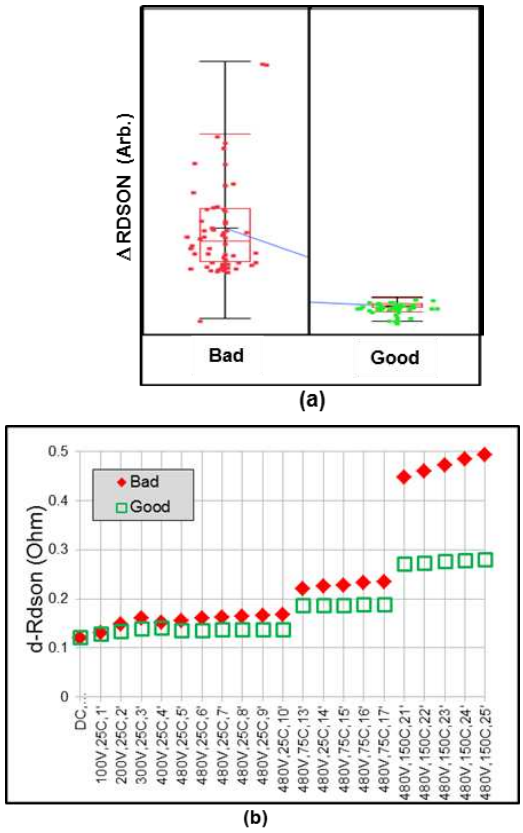

Figure 4 Screening results of high and low R_{DSON} shifters using Test A[(a)] and their corresponding continuous dynamic R_{DSON} characterization [(b)]. Note that both 75 ºC and 150 ºC tests have 480V stress only.

CONCLUSIONS

An innovative method to filter out potentially unstable and unreliable R_{DSON} shifters after long-term stress is demonstrated in GaN-based power devices. The screened data is well-correlated to the long-term stability in terms of R_{DSON} performance. The described method can identify and predict the long-term instability of high-voltage GaN-on-Si heterostructure field effect transistors in an actual application environment.

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