Hot-Phonon Effect on the Reliability of GaN-Based Heterostructure Field-Effect Transistors

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INTRODUCTION

GaN-based heterostructure field effect transistors (HFETs) are among the most promising devices for high power radio frequency (RF)/microwave (MW) and switching applications owing to their high breakdown voltage, high electron density, and high electron saturation velocity.[1,2] In fact, GaN HFETs are currently employed in RF/MW high power amplifiers, low-noise amplifiers (LNA), and RF switching modules in radar and electronic warfare (EW) systems.[3] However, reliability is still an issue to be addressed since GaN-based technology has not yet reached its maturity. Hence, addressing the physical mechanisms behind relatively poor reliability of the GaN-based crystal structure is imperative along with the empirical analyses of conventional reliability data collected from device tests such as accelerated life tests.

Joule heating is considered the main culprit that accelerates the degradation of power devices. The mechanism simply relies on energy of the electrons increasing due to the high electric field and dissipating it through electron–phonon scattering. Since hot electrons do not cool down through the interaction with acoustic phonons, emission of optical phonons dominates the phonon population at elevated power levels. Therefore, emitted optical phonons accumulate, and hot-phonon effects become significant in the GaN crystal structure, especially around the channel.

Optical phonon-associated heat cannot reach the heat sink efficiently due to the low group velocity unless they are converted to acoustic phonons. Therefore, the main avenue for device heat dissipation includes emission of longitudinal optical (LO) phonons by hot electrons, decay of the LO phonons into longitudinal acoustic (LA) phonons, and diffusion of the excess LA phonons into the remote heat sink. Moreover, the hot-electron and hot-phonon temperatures were shown to be approximately equal meaning that they constitute an almost isolated hot subsystem formed in the channel, and the bottleneck for the dissipation was caused by slow decay of hot phonons into LA phonons. This concept of the power dissipation bottleneck is highly important for power HFET operation.

Hot-phonon lifetime quantifies this type of mechanism, which is throughly visited for III-V systems such as GaAs and GaN both at low and high electron densities. At high electron densities such as in a GaN two-dimensional electron gas (2DEG), another phenomenom manifests itself which is called plasmon assisted decay of hot phonons. As the bulk density of electrons approaches near 10^{19} cm^{-3} the plasma frequency and optical phonon frequency cross over and the phonon lifetime exhibits the lower value. This finding drives the hypothesis that if phonon-plasmon coupling leads to lower phonon life-time, then devices should perform better around some certain resonant 2DEG density since the joule heat dissipation to the heat sink is more efficient by intrinsic device design.[4-13]

In this paper we selected a particular InAlN/GaN-based HFET structure as a test bed since two-dimensional electron gas (2DEG) densities reach up to $3x10^{13}$ cm^{-2}. [14-16] As an hypothesis, this presumably allows us to monitor the aforementioned resonant 2DEG density value at which the heat removal expected to be maximum.

EXPERIMENTAL

The InAlN/AlN/GaN structure was grown on a c-sapphire substrate in a metalorganic chemical vapor deposition system. The HFET structure consisted of a 250 nm AlN initiation layer grown at ∼1030 °C, 3 μm of undoped GaN deposited at ∼1000 °C, a 1 nm AlN spacer layer grown at 1000 °C, a 20 nm $In_{0.15}Al_{0.85}N$ barrier layer grown at 800°C, and a 2 nm GaN cap layer grown at 900°C. The Ti/Al/Ni/Au Ohmic contacts for the HFET devices were fabricated and mesa isolation was performed in a SAMCO inductively coupled plasma etcher based on Cl chemistry. Finally, standard liftoff procedure was used to form the Pt/Au gate electrodes (thickness 30/50 nm, length/width 2/90 μm).

Three different techniques were utilized to study the effect of degradation regarding the hot-phonon effect as follows: DC current-voltage (I-V) characteristics, current-transient

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measurements and low-frequency phase noise (LFPN) measurements. The current transient and standard DC I-V characteristics were monitored using a Keithley 4200 parameter analyzer. LFPN measurements were conducted using an Agilent phase noise setup for which the detailed description can be found elsewhere.[17]

RESULTS

Devices were selected among nearly identical devices from the same wafer, based on their current densities, transfer properties, and leakage currents measured using standard DC characterization methods. The maximum dispersion in the current density of the selected devices was about 0.06 A/mm, which corresponds to a 5% variation. The threshold voltage was about -6.8 V. A maximum 2DEG density of $2.3x10^{13}$ cm^{-2} was obtained from Hall effect measurements; the minimum density was assumed to be zero at the pinch-off condition in biased HFETs. These two values and I_D vs. V_{GS} plots were used to estimate the 2DEG density as function of gate bias. All devices were subjected to a 7 h DC stress at V_{DS}=20 V at different gate voltages.

In Fig 1 (a), two nearly identical HFETs according to their DC properties have undergone DC on-stress at two different gate bias conditions corresponding to different 2DEG density values. The profile for DC current results after stress was remarkably different for the HFETs tested. For totally open gate where the 2DEG density is maximum, drain current loss was much higher and the I-V curve was qualitatively different when compared to the one stressed at some negative gate bias. For the former, stress causes some gate-lag (open circles) in addition to the severe drain-current drop compared with the devices stressed at a lower 2DEG density (closed diamonds) for which we observed relatively mild current drop. To understand this effect better we picked several gate bias points from fully open gate to a totally closed gate where 2DEG density corresponded to its maximum and minimum values, respectively. In Fig. 1(b), we see the change in drain current, ΔI_D, measured at V_{DS}=5V and V_{GS}=0V, after the electrical stress at V_{DS}=20 V for different gate biases. Data showed that minimum degradation takes place when the gate voltage during the stress has corresponded to the resonant 2DEG density of $0.92x10^{13}$ cm^2. The current loss is below 20% at the resonance, whereas the loss was above 60% for HFETs stressed at zero gate bias when the electron density in the channel during stres was maximum and away from the resonance point. It should be noted specifically that at lower electron densities (lower than the resonant 2DEG density, n_s $< 0.92x10^{13}$ cm^{-2}), the degradation is worse in spite of lower drain current. Therefore, on both sides if bias condition shifted away from the apparent resonant 2DEG density, current loss due to stress degradation increases.

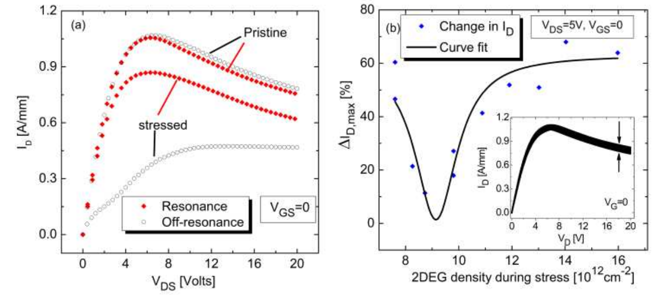


Fig. 1 (a) A representative I_D vs. V_{DS} graph measured at zero gate bias for two HFETs before and after the stress at V_{DS} = 20 V when the gate was biased to the hot phonon–plasmon resonance (closed diamonds) and at the off-resonance (open circles). (b) Change in drain current ΔI_D due to the stress at V_{DS} = 20 V as a function of 2DEG density during stress and the Lorentzian fit (Inset) Drain current vs. drain-source voltage for the devices used. A dispersion of five percent was observed among the maximum drain current values of the selected devices.

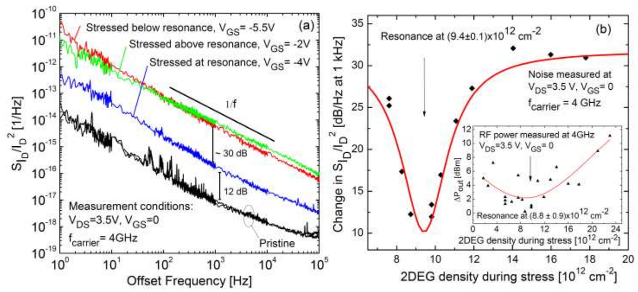


Fig. 2 (a) Normalized noise data for resonant and off-resonant 2DEG densities under stress. (b) Increase in the noise measured at zero gate bias after 7 hr electrical stress at 20V drain bias as a function of channel 2DEG density during stress controlled by the gate bias. The clear resonance is observed at a 2DEG density around $0.94x10^{13}$ cm^{-2} (fitting line) corresponding to the minimum degradation. The inset shows the reduction in the RF output power (ΔP_{out}) at 4GHz after stres with the fit guiding the eye. The arrows mark the resonant 2DEG density.

We also monitored phase noise for each device relative to a 4 GHz carrier signal using an Agilent 5505 test set. More details on this particular technique can be found in Refs. 17–19. Fig. 2 (a) shows the representative noise data in normalized power spectral density (PSD) units. We noted the change in normalized PSD at 1 kHz as a function of the 2DEG density (under stress) for different gate biases (Fig. 2 (b)). The pristine devices exhibited almost identical noise spectral densities. The stress condition corresponding to the resonant 2DEG density (V_{GS}= -4V) yielded a 12 dB increase in the noise power, whereas the completely off-resonant stress conditions (V_{GS}= -2V and V_{GS}= -5.5V) exhibited an increase of about 30 dB. The trend of normalized noise data strongly correlates with that of the ΔI_D data [(Fig. 1(b)]. A sharp resonance is resolved at a sheet density around $0.94x10^{13}$ cm^2 (fitting line). This value is consistent with the values of $0.92x10^{13}$ cm^{-2} and $0.93x10^{13}$ cm^{-2} obtained from Fig. 1(b) and current-gain-cutoff-frequency measurements at high fields [20], respectively. The devices exhibit dramatically higher normalized PSD values in the range from 12 dB/Hz to 32 dB/Hz after being subjected to the stress at V_{GS}= -4V and V_{GS}= -2V, respectively. On the left-hand side of the resonance, the noise increases up to 28 dB/Hz at V_{GS}= -5.5V. Compared to the stress at the resonant conditions, the HFETs stressed at completely off-resonant 2DEG densities exhibit up to 16–20 dB higher noise values for the left-hand and the right-hand sides of the resonance, respectively. The reduction in the RF power output (ΔP_{out}) at 4 GHz carrier frequency was also plotted as a function of 2DEG density during the stress in the inset of Fig. 2 (b). The results support the noise data: the devices stressed at a given gate bias demonstrate the minimum power loss at the same optimal 2DEG density.

Along with the previous two measurement techniques, we tested HFETs through their transient behaviors in the context of degradation as a function of 2DEG density. Fig. 3 displays the transient drain currents of three different HFETs before and after electrical stress. All transients were obtained at V_{DS}= 7 V and with a pulse depth of -7V. In Fig. 3 (a) and 3 (c), we plotted transients of representative HFETs stressed at bias parameters corresponding to 2DEG densities above and below resonance, respectively. A remarkable permanent degradation was observed for both, at about 60 % for above resonance and 50 % for below resonance. However, devices stressed at resonant-2DEG-density conditions exhibited much less degradation (about 6 %, see Fig. 3 (b)) compared with the off-resonant stress conditions. These results from transient current measurements are consistent with the I-V and LFPN measurements (Fig. 1b and Fig. 2b, repectively). Moreover, post-stress pulsed measurements exhibited a loss of 80% and 63 % in the drain current for devices above and below resonant-2DEG-densities, respectively, whereas the loss for HFET stressed at resonant-2DEG-density was only 16 %. Recovery rates for all pulsed measurements were negligible within the measurement time span up to 5ms.

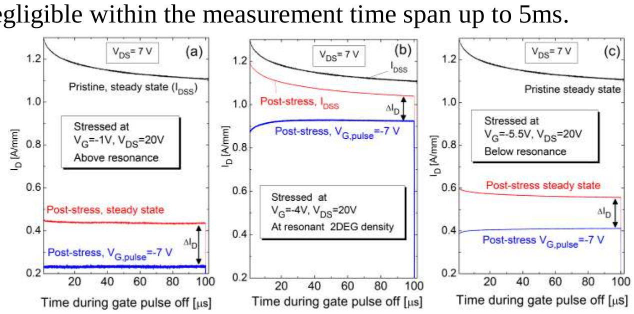


Fig. 3 (a) Current transient of a device stressed at off-resonant conditions for which the 2DEG density is higher than the resonant 2DEG density value. There is a remarkable permanent degradation about 60 %. Post-stress pulsed measurements exhibited almost total loss of the drain current (80 %). (b) Transient data for the device stressed at resonant 2DEG conditions yielded a much lower degradation and trapping effect. (c) Device stressed at the off-resonant conditions at which the 2DEG density is lower than the resonant 2DEG density exhibited high degradation (50 %).

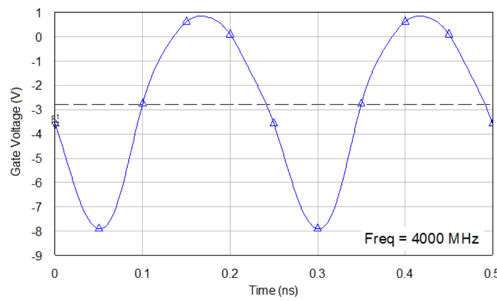
DISCUSSION

Direct current-voltage (I-V), low-frequency phase noise, and transient current measurements showed the existence of a point at which the device degradation is minimum as a function of apparent 2DEG density. We suggest the following account for this result: The hot-phonon build-up phenomenon at off-resonant bias conditions causes both the drain–gate access region degradation and trap generation in the barrier and buffer due to abovementioned thermally isolated subsystem of hot electrons and hot-phonons.

The stronger hot-phonon associated degradation at off-resonant operation manifests much higher noise caused by either electron number, mobility fluctuations, or both [17-19]. At resonance, the lower degradation of the GaN channel quality and mild deep-trap generation in the buffer layer can be responsible for the higher noise and stronger drain-current drop. [21] However, at off-resonance conditions, up to 30 dB higher noise (Fig 2) was caused by carrier number fluctuation as a result of trap generation in the barrier and buffer layers as well as the amplified mobility fluctuations due to the damage in GaN-channel.

Considering the transient current results (Fig. 3), temporary collapse of drain current in stressed devices having long recovery times may be directly associated with the deep traps generated during the electrical stress process. However, the permanent loss in drain current may be attributed to the channel quality damage on the drain side of the gate. In addition, the difference between pulsed and steady state currents may be the direct evidence of the discrimination between bulk/barrier-trap related degradation and severe channel damage.

Nevertheless, commercial HPA/MMIC technology employs AlGaN/GaN structures instead of InAlN/GaN-based ones. How would hot-phonon phenomenon in the context of abovementioned results affects degradation for AlGaN/GaN system? This question can simply be addressed as follows: Since the 2DEG is formed in the GaN side of the AlGaN/GaN interface, it is expected to have a similar resonant 2DEG density at which the degradation is lower. An AlGaN/GaN heterojunction has sheet electron densities of about $0.8\text{-}1.1\times10^{13}$ cm^{-2} at zero gate bias depending on the Al composition in the barrier region. This sheet density is lower than the InAlN/GaN interface sheet density. Surprisingly, this value is intrinsically around the resonant sheet density at zero gate bias. However, when RF drive is applied, the quiescent point is usually kept very close to pinch-off, where RF swing creates an effective voltage as seen in Fig. 4. Regarding the drain current values for an HPA operating under RF drive, a first-order-approach estimate shows that an effective bias point corresponding to a sheet density of about $0.3\text{-}0.4\times10^{13}$ cm^{-2}. This value seems to be a little far from the resonant sheet density (0.94×10^{13} cm^{-2}) at which the device operates at a lower temperature, where reliability could be improved. AlGaN/GaN-based devices should be tested during RF operation to confirm the effect of hot-phonons further on the reliability of HPAs.



CONCLUSIONS

Low-frequency phase-noise measurements, DC current vs. voltage results, and current transient measurements on InAlN/AlN/GaN HFETs show that device degradation is lower at the resonant 2DEG density of $0.94x10^{13}$ cm^{-2} than at off-resonant conditions. This sheet density value is also consistent with the resonances observed in small signal RF measurements. Overall, the results are consistent with the phenomenon of hot-phonon build-up and ultrafast decay due to the phonon–plasmon coupling at the resonant 2DEG density. Further measurements and anylses are needed in order to confirm hot-phonon effect on degradation of high power devices under RF drive.

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ACRONYMS

HFET: Heterostructure Field-Effect Transistor
RF: Radio Frequency
MW: Microwave
LNA: Low Noise Amplifier
2DEG: Two-dimensional Electron Gas
LFPN: Low-frequency Phase Noise
PSD: Power Spectral Density
HPA: High Power Amplifier
MMIC: Monolithic Microwave Integrated Circuit