Effect of Gate Threshold Swings by ALD-Al_2O_3/AlGaN Interfacial Traps in GaN Power HEMT with Multiple Fluorinated Gate Dielectric Layers

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Abstract

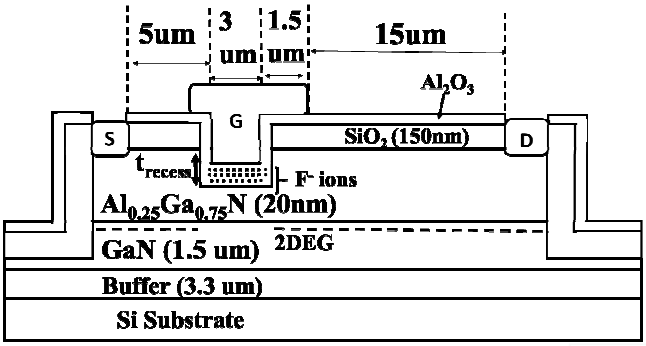
This work analyzes the Al_2O_3/AlGaN interfacial quality of annealing-free device with multiple fluorine plasma treatments within Al_2O_3 gate dielectric in HEMT which is expected to have good channel conductivity and high V_{TH} at the same time. Benchmarking with devices that underwent pre-fluorination annealing right after 1st layer of Al_2O_3 deposition, unannealed device has about 10 times lower shallow interface trap density (D_{it}) which resulted in significantly smaller drain leakage current. However, doubled Ultra-violet (UV) -assisted V_{TH} hysteresis (ΔV_{TH}) in bi-directional I_D-V_G sweep measurement indicates higher concentration of deep-level traps without gate stack annealing.

INTRODUCTION

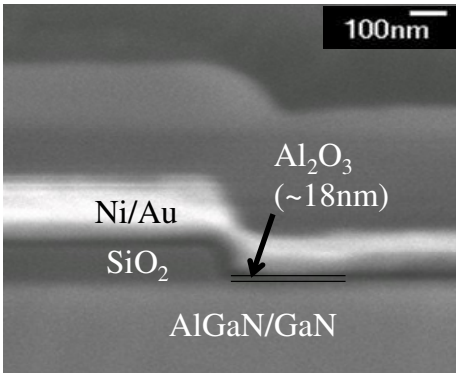
Normally-off AlGaN/GaN HEMT is desirable in power applications in terms of system controllability. Fluorine ion (F^-) treatment [1] and AlGaN barrier recess [2] on the gate region are both approaches to deplete the carriers or weaken the polarization within the normal 2DEG conduction channel in HEMT structure. However, for conventional F^- treatment on AlGaN surface [1], annealing was required after treatment for damage recovery which resulted in the migration of F^- and reduced V_{TH}. Unannealed multiple F^- treatments on AlGaN surface and ALD-Al_2O_3 gate dielectric combining with partial AlGaN recess reported in [3] allowed high total amount of F^- incorporation at the gate which resulted in a high V_{TH} of +5V.

DEVICE FABRICATION

The HEMT device fabrication on the AlGaN/GaN-on-silicon wafer begins with Ti/Al/Ni/Au (25/125/45/55 nm) ohmic contacts formed by RTA at 850°C for 30s. Then, 500nm-deep mesa isolation is formed by BCl_3-based ICP-RIE and 150nm SiO_2 dielectric deposition by PECVD. After gate opening, about 10nm of AlGaN (50% in thickness) was recessed by low power BCl_3-based ICP-RIE to weaken the polarization and reduce the 2DEG concentration without degrading the AlGaN/GaN 2DEG interface mobility. After 6.5nm of ALD-Al_2O_3 deposition at 250°C and different post-deposition annealing temperatures for gate recess recovery used on Dies B and C, 3 cycles of CHF_3 plasma treatment combining with ALD-Al_2O_3 were used for gate stack formation to introduce sufficient F^- charges in the gate region for high V_{TH}. Longer treatment period was applied on the top layer to minimize F^- penetration into the 2DEG channel region which may create mobility degradation. Considering the CHF_3 plasma etching on Al_2O_3, the total Al_2O_3 thickness of 18.1nm is obtained. Detailed device schematics, SEM of the gate cross-section and gate process parameters are shown in Fig. 1 and Table I. The equivalent F^- sheet concentration of each layers was obtained by fitting the measured V_{TH} with Setaurus TCAD simulations.



(a)



(b)

Fig. 1 (a) Cross-sectional schematics and **(b)** SEM image of the fabricated device

Table I. Steps for gate fabrication of Dies A~C

Steps	Process	Dies		
		A	B	C
1	ALD-Al_2O_3	6.5 nm		
2	Rapid thermal annealing	N/A	500 °C in N_2 for 60s	600 °C in N_2 for 60s
3	F^- treatment	CHF_3 RIE @ 30W for 140s F^- Conc.~= -6.51×10^{12} cm^{-2}		
4	ALD-Al_2O_3	7.3 nm		
5	F^- treatment	CHF_3 RIE @ 30W for 260s F^- Conc.~= -1.21×10^{13} cm^{-2}		
6	ALD-Al_2O_3	7.6 nm		
7	F^- treatment	CHF_3 RIE @ 30W for 280s F^- Conc.~= -1.30×10^{13} cm^{-2}		
8	ALD-Al_2O_3	8 nm		
Total Al_2O_3 thickness after F^- RIE treatment (nm)		**18.1 nm**		

RESULTS AND DISCUSSION

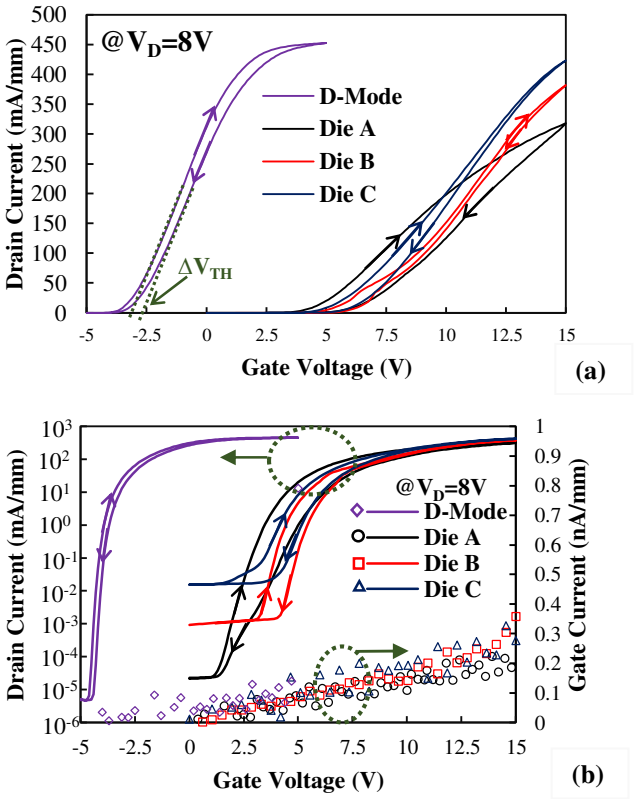


Fig. 2 (a) Bi-directional transfer characterisic of Dies A-C with benchmarking D-mode device in linear scale. The sweep was done in 20s and threshold voltage hysteresis (ΔV_{TH}) is demonstrated. **(b)** Bi-directional transfer characterisic in logarithmic scale and I_G-V_G characteristics of Dies A-C and D-mode device. Low gate leakage current has ensured the preservation of insulation quality of the gate dielctric with fluorine treatments.

Fig. 2 (a) shows the bi-directional transfer characteristics (sweep time=20s) of Dies A~C at V_D=8V comparing with D-mode MIS-HEMT with Al_2O_3 of 18nm without any gate recess. Slight increase of V_{TH} in positive sweep were found with annealing (step 2 in Table I), showing the formation of some fixed negative charge after annealing. Additionally, different degree of positive shift in V_{TH} was observed during negative sweep, indicating trapping of electrons at the Al_2O_3/AlGaN interface or Al_2O_3 bulk after applying high gate bias. Halved ΔV_{TH} was observed after annealing, proving effective reduction in deep-level Al_2O_3/AlGaN interfacial trap charge (Q_{it}). Shown in Table II are Q_{it} values for Die A~C based on Fig. 2(a) along with the Q_{it} values after 10s of UV-illumination (UV wavelength=365nm) to measure even deeper Al_2O_3/AlGaN traps. Q_{it} were extracted according to [4] as shown in Eq. (1). In Eq. (1), ε_{Al2O3}=7, ε_0 is the permittivity in vacuum, q is the electronic charge and t_{Al2O3} is the thickness of Al_2O_3 as shown in Table 1. The bi-directional I_D-V_G in log-scale and I_G-V_G shown Fig. 2(b) has demonstrated increased drain leakage current under similar gate leakage after annealing.

$$Q_{it} = \frac{\varepsilon_0 \varepsilon_{Al_2O_3} \Delta V_{TH}}{q t_{Al_2O_3}} \quad (1)$$

Table II. Extracted threshold voltage hysteresis and Al_2O_3/AlGaN interfacial trap of Dies A~C.

Dies		D-Mode	A	B	C
V_{TH} in positive sweep (V)		-3.0	4.8	5.4	5.5
w/o UV	ΔV_{TH} (V)	0.4	1.4	0.75	0.5
	Q_{it} (10^{12} cm^{-2})	0.86	3.01	1.61	1.08
UV for 30s	ΔV_{TH} (V)	0.4	2.0	1.25	1.00
	Q_{it} (10^{12} cm^{-2})	0.86	4.40	2.72	2.20

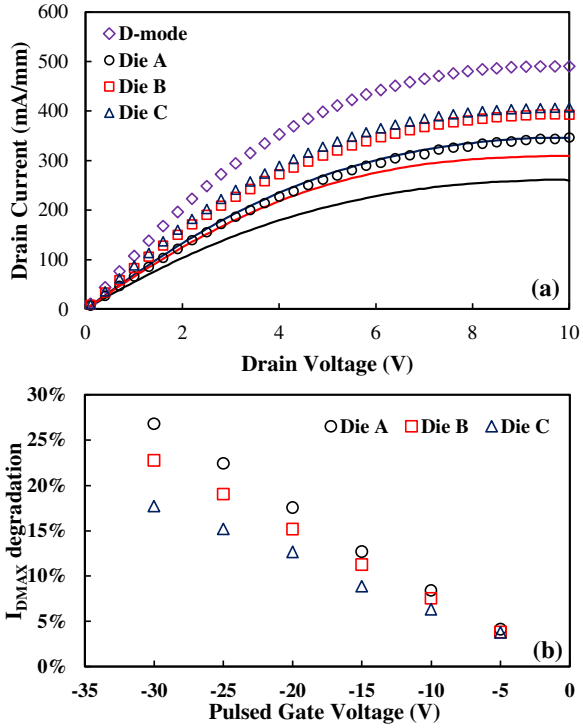


Fig. 3 (a) I_D-V_D characteristic of Dies A-C with benchmarking normally-on device at gate drive voltage in excess of V_{TH} (V_{GT}) of 10V in DC state (datapoints). Pulsed I_D-V_D (solid line) measured

with V_G pulse for 50ms swithing between -30V and V_{GT} = 10V with 50% duty cycle is also included. High I_{DMAX} of 350 mA/mm was found for Die A, showing effectiveness of annealing on mobility restoration; **(b)** The amount of I_{DMAX} degradation for pulsed I-V measurement compared with DC I-V results at different pulsed gate voltage. Alleviation in the current collapse effect is found for Die C.

Fig. 3 (a) compares the DC and pulsed I_D-V_D characteristic of Dies A-C at gate overdrive voltage (V_{GT} = V_G -V_{TH}) of 10V. For Pulsed I_D-V_D, it was measured with V_G pulse at −30V for 50ms and 50% duty cycle to examine the current collapse effect due to deep-level trapping of electrons from gate injection to the trap sites within the gate dielectric, at the Al_2O_3/AlGaN interface, or along the surface. High I_{DMAX} of 350mA/mm from unannealed Die A under steady state has shown good preservation of 2DEG mobility after CHF_3 plasma treatment. In Fig. 3 (b), similar I_{DMAX} degradation was found for Die A, B, and C under small pulsed negative V_G, showing similar amount of trapped electrons since they are injected near the device surface. When pulsed V_G is large enough to inject electrons into the Al_2O_3/AlGaN interface, worse current collapse effect is for Die A compared with Die B and C due to absence of annealing to recover the etch damage. The worse I_{DMAX} degradation under high pulsed V_G agrees with the higher amount of deeper level traps shown in Table II.

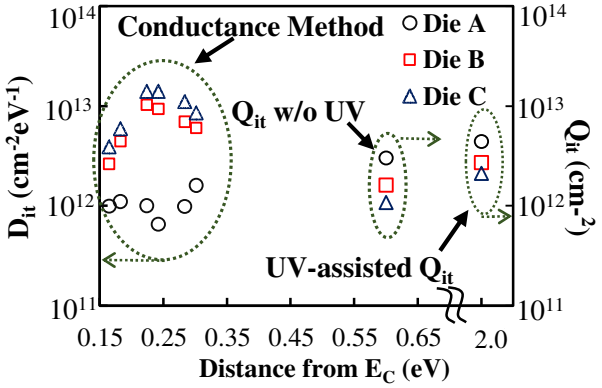
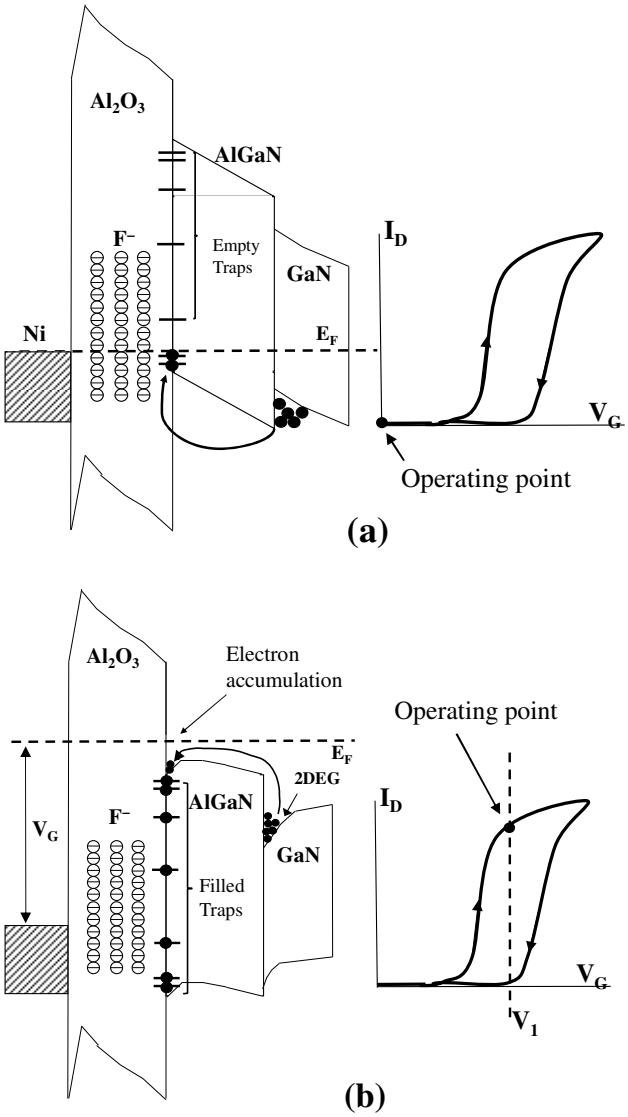


Fig. 4 Al_2O_3/AlGaN interface trap density (D_{it}) distribution within the AlGaN energy band obtained from conductance method (E_T=0.165 eV to 0.3 eV) and trapped interface charge Q_{it} from Bi-directional transfer characteristics before (E_T=0.6 eV based on 20s I_D-V_G sweep rate) and after 10s UV lamp illumination (E_T=2 eV) shown in Table II.

Fig. 4 shows the Al_2O_3/AlGaN interface trap density (D_{it}) distribution from the AlGaN E_V edge obtained from AC conductance method using Eq. (2) [5]. In Eq. (2), $(G_p/\omega)_{max}$ is the maximum value of the ratio between the parallel conductance (G_p) and the frequency in radians (ω) at each measured frequency, and A is the area of the gate. The corresponded trap energy level (E_T) from the conduction band edge to the frequency used in C-V measurements is given by the Schottky-Read-Hall statistics shown in Eq. (3) [5]. In Eq. (3), k_b is the Boltzmann's constant, T is the ambient temperature, f is the characterized frequency, σ is the capture cross-section of the trap, which is about 3.4×10^{-15} cm^2 [6], υ_{th} is the average thermal velocity of electrons (about 2.6×10^7 cm/s), and D_{dos} is the effective density of states of electrons within AlGaN, which is about 3.3×10^{18} cm^{-3} [6]. Annealing would increase the shallow trap level (E_T) density near the E_C edge by about a factor of ten, while the deeper-level Q_{it} obtained before (E_T=0.6eV based on 20s I_D-V_G sweep rate) and after (E_T=2eV, mid-gap of AlGaN) UV illumination with wavelength of 365nm for 10s shown in Table II decreases with raised annealing temperature.

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{max} \quad (2)$$

$$E_T - E_C = k_b T \ln(2\pi f \sigma \upsilon_{th} D_{dos}) \quad (3)$$



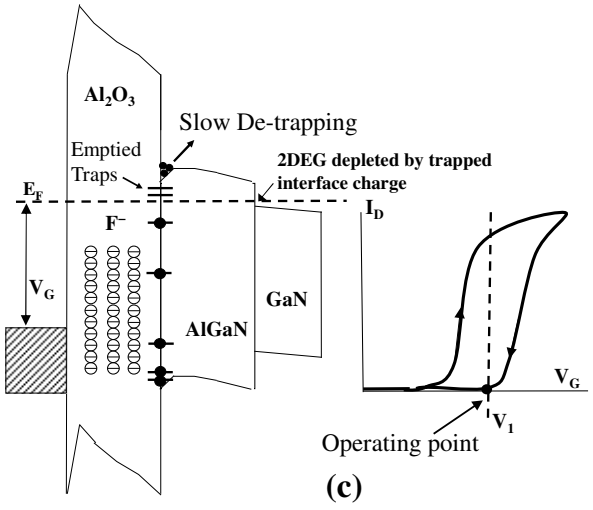


Fig. 5 Schematic energy band diagram of Al_2O_3/AlGaN/GaN interface at **(a)** V_G=0V (leakage current induced by hole trapping in shallow D_{it} and hopping across the gate region into the channel) **(b)** V_G=V_1 in positive sweep (trapping of Q_{it} from 2DEG) and **(c)** V_G=V_1 in negative sweep (2DEG depletion from Q_{it} resulted in positive V_{TH} shift)

Fig. 5 explains the effect of carrier trapping & de-trapping mechanisms on ΔV_{TH} through schematic energy diagram. In Fig. 5 (a) when V_G=0V, holes accumulated at AlGaN/GaN interface will be trapped at the shallow Al_2O_3/AlGaN trap levels and hopping across the gate region into the channel induces drain leakage current. More shallow level traps were found for annealed dies shown in Fig. 4 explains greater drain leakage current for Dies B & C shown in Fig 2(b). When V_G>V_{TH}=V_1 in positive sweep shown in Fig. 5(b), electrons from 2DEG will be trapped at Al_2O_3/AlGaN interface. Those trapped electrons will be slowly de-trapping back into 2DEG during negative sweep and those charges remained at the Al_2O_3/AlGaN interface will deplete the 2DEG that causes positive V_{TH} shift under the same gate bias V_1 shown in Fig. 5(c). Thus, a higher amount of deep-level traps will result in greater trapped charges and larger ΔV_{TH} during the negative sweep.

CONCLUSIONS

In this paper, the Al_2O_3/AlGaN interfacial quality for fluorinated Al_2O_3 gate dielectric with triple CHF_3 based plasma treatment has been verified. It is found that pre-fluorination annealing on the base layer Al_2O_3 decreased the amount of deeper level interfacial traps attributed to the V_{TH} hysteresis when carrying out bi-directional I_D-V_G sweep. However, shallower trap concentration increased, which resulted in higher off-state drain leakage current.

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ACRONYMS

HEMT: High Electron Mobility Transistor
ALD: Atomic Layer Deposition
PECVD: Plasma Enhanced Chemical Vapor Deposition
SEM: Scanning Electron Microscope
MIS-HEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor
ΔV_{TH}: Change in V_{TH}