6-inch VCSEL Wafer Fabrication Foundry Economics

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Abstract

The way we interact with the world around us is poised to change, as advanced sensing capabilities are being designed into a multitude of consumer electronics devices. VCSELs offer the right performance and manufacturability in support of this trend, but are currently not scalable to the volumes and cost structure required. Migrating to 6-inch wafer fabrication effectively solves these challenges.

INTRODUCTION

The VCSEL was demonstrated in 1979, but devices for operation at room temperature were not developed until ten years later. As device design, epitaxial material and wafer processing components evolved in vertically integrated manufacturing systems, VCSELs increased in performance, reliability and availability. With better economics, manufacturability, packaging and testing, GaAs-based VCSELs started to replace edge-emitting lasers in applications for short-range fiber optics communications, including Gigabit Ethernet and fibre channel and optical mice.

While GaAs-based VCSELs have revolutionized data communications systems by providing a low cost, high-volume manufacturing platform, the emerging trend is to use these devices as near infrared illumination sources to replace LEDs. Sensing, gesture recognition, biometrics and free-space optics are being adopted in a variety of markets, including entertainment, mobile computer and automotive. For example, Princeton Optronics Inc, a US-based manufacturer of Vertical Cavity Surface Emitting Lasers (VCSEL) and VCSEL arrays, recently announced that the company is working with Google's Advanced Technology and Projects group (ATAP) on the development and deployment of compact mobile imaging systems that will enable users to interact with their environments in three dimensions. This trend is placing pressure on the current manufacturing infrastructure to significantly reduce cost and increase capacity.

MANUFACTURING CHALLENGES

Consumer electronics devices are often manufactured at an incredible rate. From smartphones to tablets to gaming systems, billions of these devices are shipped each year. The inherently better performance of VCSELs compared with LEDs and the desire to embed greater sensing capabilities is driving manufacturers to select VCSELs for their newest consumer electronics designs. However, the key to VCSELs successfully displacing LEDs is to be able to manufacture them with the same scale, quality and cost structure.

Most existing VCSEL manufacturing occurs on 3-inch diameter substrates, which were developed to support data communications and specialty applications that utilize small die. With substantially higher volume applications and a larger die size, the ability to add capacity and scale to meet production requirements is critical for new large volume end applications. This challenge is further exacerbated by the implementation of VCSEL devices in consumer applications. To meet the performance requirements of these applications, there is a greater demand for arrays of VCSEL emitters, increasing the die size.

MANUFACTURING SOLUTION

To meet the needs of these new applications, VCSEL manufacturing capabilities need to scale in a manner similar to the transition of GaAs RF products when substrates increased from 3-inch to 4-inch and then to 6-inch diameters. A 6-inch GaAs VCSEL platform provides 400% the wafer area of a 3-inch wafer and at least that many more die on each wafer. When comparing any increase in wafer diameter, the incremental production cost, epi material plus wafer processing, needs to be low enough to allow a cost benefit, assuming similar manufacturability and yields. As in all other semiconductor manufacturing scenarios, a larger diameter wafer provides the most compelling economics.

So critical and time-sensitive are these optical systems that the US government has recently announced a photonics manufacturing initiative to scale production capacity, reduce component costs and assure a stable, US-based supply chain. 6-inch VCSEL production uses a more advanced wafer fabrication tool set and epi growth systems that provide better cross-wafer uniformity, controllability and ultimately better yields and costs.

Similar to RF GaAs product manufacturing, the 6-inch VCSEL platform is more economical because the epi wafer starting material and processing are more cost effective.

The wafer size is critical in the ROI and cost calculations of the foundry model. Moving to a 6-inch platform increases the wafer usage beyond the area scaling due to edge exclusion regions of the wafer. That also becomes more significant as the die size increases because there are fewer die lost at the wafer edge. The 6-inch wafer provides 460% the usable wafer area compared to a 3-inch wafer, and 240% usable wafer area compared to a 4-inch, wafer when a typical 5 mm edge exclusion is considered. This all results in greater cost efficiency as the die get larger as shown in Table 1 which reflects perfect timing for these new applications with large arrays and high volumes.

Increase compared to 3-inch wafer	*6-inch wafer benefits*
4X area increase	3-inch to 6-inch diameter
4.6X usable wafer area	With 5mm edge exclusion region
4.7X – 5X GDPW	For larger die

Table 1: Summary of 6-inch wafer benefits and resulting die increase

The most cost effective manufacturing approach is to maximize the gross die per wafer (GDPW). The GDPW is compared in Figure 1 for various die sizes across 3-inch, 4-inch and 6-inch substrates. For comparison, the relative GDPW is shown for a single die (0.25 mm x 0.25 mm), a 4-channel array (0.25 mm x 1.0 mm), a 12-channel array (0.25 mm x 3.0 mm), a 2-D array (1 mm x 1 mm) and a large 2-D array (2 mm x 2 mm).

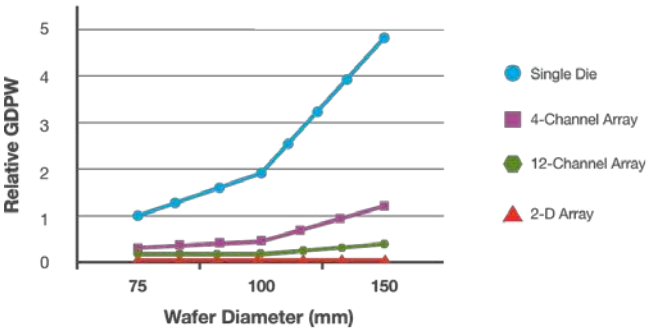

Figure 1: Relative GDPW for various VCSEL die sizes on 3-inch, 4-inch and 6-inch substrates

In addition to using a larger wafer to increase GDPW, the usable wafer area is also important for large die sizes. The usable area of a 3-inch wafer can be less than 90% for large die and can be increased to close to 95% on a 6-inch wafer. This results in a cost improvement of up to 6% based on the usable die area as the die size increases as shown in Figure 2. The effect of the die aspect ratio and edge exclusion is demonstrated by the larger utilization of a 2-D array than a 12-channel linear array.

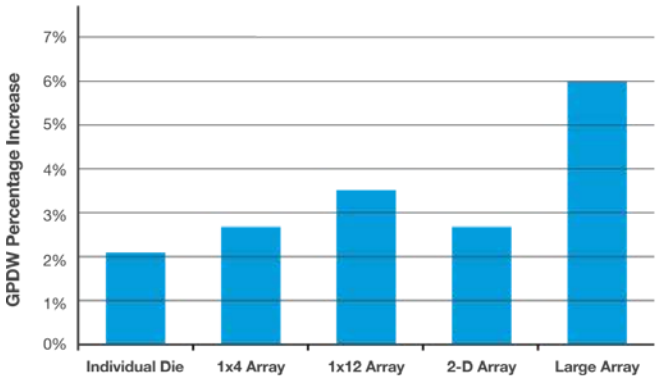

Figure 2: Wafer usage increase from 3-inch to 6-inch substrates for various VCSEL die sizes

DEVELOPING A 6-INCH PROCESS

Migrating to a 6-inch manufacturing process starts with the process development. ANADIGICS has expertise in these fundamental process technology advancements -- launching the first 6-inch RF GaAs fab in 1999. The Company leveraged this experience to develop the world's first 6-inch GaAs-based VCSEL process. During that transition, additional manufacturing efficiencies and cost improvements were discovered due to the more advanced 6-inch tool set.

The economic drivers of the 6-inch foundry include the larger wafer size, expandable fabrication capacity and scalable test capabilities. In order to provide a complete solution, it is important to build out the entire supply chain network. Concurrent with developing wafer fabrication capabilities, 6-inch VCSEL epitaxial wafers were introduced into the market. In fact, IQE plc announced availability of these materials in March 2014. In addition to the epi material and wafer fabrication capabilities, increased test capacity is also key to enabling these applications. High volume GaAs RF wafer level test strategies and infrastructure can also be leveraged on a 6-inch manufacturing platform.

VCSEL FOUNDRY APPROACH

The foundry model provides scalable capacity with low investment costs to optimize productivity and costs. The VCSEL wafer foundry approach has been demonstrated, though most VCSEL device manufacturers are still vertically integrated. Until now, product demand did not justify the investment costs and operating expenses of a 6-inch VCSEL platform. New applications with different cost and volume requirements require that VCSEL manufacturing scale to a 6-inch platform to provide additional manufacturing efficiencies.

There are three different approaches to VCSEL fabrication: 1) fully integrated device manufacturing (no foundry), 2) fabless manufacturer (all foundry) and 3) fab-lite manufacturing (combination of internal and external fab). Since VCSEL products require a unique combination of epi material, device architecture, fabrication techniques and product design, there is little way to differentiate products simply by the design, as is common in other merchant foundries. Because of this, the VCSEL foundry approach uses a custom foundry model that does not employ standard device libraries or standard cells for all customers to use. Each customer defines a wafer fabrication process unique to the product. The VCSEL custom foundry allows device manufacturers to optimize device and processes for individual applications with unique requirements, while utilizing all of the foundry model advantages. This is similar to the vertically integrated device manufacturer approach and can be employed in any of the manufacturing scenarios.

The foundry model allows all manufacturers access to, in the case of 6-inch wafers, a more advanced tool set and scalable capacity. There is very little investment required to develop or port a custom manufacturing process that can be scaled to high volume production by the foundry. When the volumes and cost structure support it, and investment resources are limited, the foundry model has been demonstrated to offer a quick and inexpensive way to address new product and market opportunities. Aggregating large volumes allows a foundry to expand process capabilities that individual fabs would find cost prohibitive. Expanding capacity is also more cost effective when a foundry can amortize tool usage over a large number of products. An example of this is the ANADIGICS investment in a high-volume oxidation furnace that supports 6-inch wafers and enables multiple process flows.

The foundry model offers additional flexibility in the business strategy, specifically in the make versus buy decision and ROI calculations. This is especially critical when considering new markets with larger volume requirements, as measured in wafer area. The fully integrated device manufacturers must consider if a particular product opportunity can be produced in the existing fab with the existing tool set, manufacturing processes and skill sets. The business decision then also considers additional capital expenditures required to bring a new product to market. The foundry model allows an additional degree of product development and manufacturing flexibility and can be combined with internal fabrication capability.

The fab-lite model provides the flexibility to address business opportunities that require costs and volumes that are not compatible with internal fabs. This also allows for prototyping and low volume production to occur internally, with a transition to the foundry when volumes or cost points require it.

CONCLUSIONS

ANADIGICS has successfully demonstrated a 6-inch GaAs VCSEL fabrication process, enabling the VCSEL foundry capabilities required to scale manufacturing in support of aggressive volume and costs requirements of new applications.

The custom foundry model using 6-inch wafer offers high volume, cost-effective and scalable manufacturing capabilities that allow VCSELs to compete in consumer applications with large die sizes.

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ACRONYMS

VCSEL: Vertical Cavity Surface Emitting Laser
GDPW: Gross Die Per Wafer