Electrical Properties of GaN Etched by Low Bias Power Process

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Abstract

We have developed low damage dry etching for fabricating recess gate AlGaN/GaN-HEMTs. In this study, simple SBD structures, which were fabricated on a GaN surface etched by ICP plasma, were used to evaluate the etching damage. To decrease the damage and inhibit the degradation of Schottky barrier height (ϕ_B), extremely low bias power etching was applied. We developed two types of etching: one with BCl_3 and the other with Cl_2/BCl_3 mixture. BCl_3 etching under low bias power condition resulted in a very rough surface. Furthermore, reduction in ϕ_B degradation due to etching could not be attained. On the other hand, the optimized Cl_2/BCl_3 etching resulted in a smooth etched surface even under low bias power condition, and thus extremely low ϕ_B degradation due to etching was realized. This low damage etching was applied to fabricate a recess gate AlGaN/GaN-HEMT with a thick AlGaN layer. This device achieved excellent performance compared to conventional device, in terms of exhibiting large maximum transconductance, large drain current, and low current collapse.

INTRODUCTION

AlGaN/GaN-HEMTs can be potentially used as high-speed and high frequency applications[1]. To improve the device performance, their on-state resistance (R_{on}) needs to be reduced. In such a case, AlGaN/GaN-HEMTs present an advantage as they have low sheet resistance (R_{sh}) owning to the use of a thick AlGaN layer. However, increasing the gate to channel distance (d_g) of HEMTs causes poor channel modulation. Therefore, the use of a recess gate structure to shorten d_g is often employed for AlGaN/GaN HEMTs. [2,3]

Cl-based dry etching techniques are generally applied to fabrication process for recess gate GaN-HEMTs. However, during dry etching, damage in the epitaxial layer often occurs due to the generation of N or Ga vacancies, diffusion of impurities, and generation of defects in crystal. This damage degrades the electrical properties of devices that are fabricated by using recess etching. This etching damage can be evaluated from some methods, such as by evaluating Schottky properties[4,5]. However, there are few reports on Schottky properties of surfaces etched under low bias power conditions.

In this study, we used simple SBD structures on etched GaN surfaces to evaluate the etching damage and tried to reduce the damage by using extremely low etching bias power. In addition, the optimized etching was employed to fabricate recess gate AlGaN/GaN-HEMTs and device characterization was performed on these devices.

EXPERIMENTAL

Si-doped n-GaN epitaxial structures were grown by MOCVD on sapphire substrates. The thickness of n-GaN and the doping concentration were designed to be 2 μm and 2×10^{17} cm^{-3}, respectively. Furthermore, n-GaN layers were etched by an ICP dry etching system. The bias power was varied from 1.5 to 20 W (the peak to peak voltage was varied from 30 to 290 V) under BCl_3 or Cl_2/BCl_3 mixture condition. In order to generate low bias power reliably, output power was reduced by an attenuator in the etching system. Etching time was adjusted to achieve an etching depth of 100 nm. Surface morphologies of the etched n-GaN were observed by AFM. Circular Ni/Au Schottky electrodes of a diameter of 400 μm were fabricated on the etched surface. Capacitance-voltage (C-V) measurements and current-voltage (I-V) measurements of the Schottky electrodes were carried out. The results of C-V measurements were used to calculate ϕ_B.

RESULTS AND DISCUSSIONS

1) BCl_3 etching

Figure 1 shows the AFM images of the GaN surface etched by our BCl_3 etching process. As shown in Fig. 1(d), great smooth surface was obtained by using BCl_3 etching with a bias power of over 10 W. However, low bias power etching tends to produce a rough surface, such as that shown in Fig. 1(b) and Fig. 1(c). It is known that some solid state boron-chlorine compounds can be generated in BCl_3 plasmas[6]. These compounds may then be deposited on the surface and inhibit etching. Such deposition might have affected the low bias power etching with a low etching rate and resulted in a rough etching surface.

Figure 2 shows dependence of normalized ϕ_B, calculated from C-V measurements, and RMS roughness on bias power

of BCl_3 process. Normalized ϕ_B was calculated from ϕ_B (post etched samples)/ ϕ_B (as-grown sample). As shown in Fig. 2, normalized ϕ_B approached 1 as bias power decreased. This result implies that etching damage is dependent on bias power. However, even though their low bias power, normalized ϕ_B at 1.5 and 3 W were lower than that at 5 W. It was considered that a rough etched surface strongly degrades ϕ_B. Therefore, both low bias power and smooth surface morphology are essential to realize low damage etching.

As shown in Fig. 3, forward current of SBDs also indicate that high power etching (10 and 20 W) cause degradation of ϕ_B. Furthermore, I-V curves obtained for 1.5 and 3 W exhibit plateaus for voltage less than 0.5 V. These plateaus presumably originated from some etch-pits generated in low bias conditions.

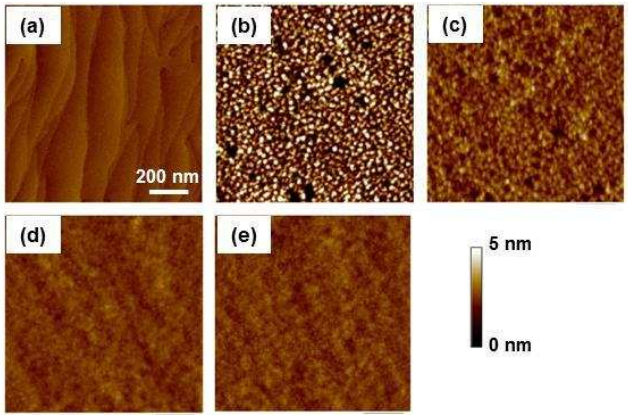

Fig. 1 AFM images of GaN surface etched by BCl_3 etching process ;(a)as-grown, (b)bias power 1.5 W, (c)bias power 3 W, (d)bias power 10 W, (e)bias power 20 W.

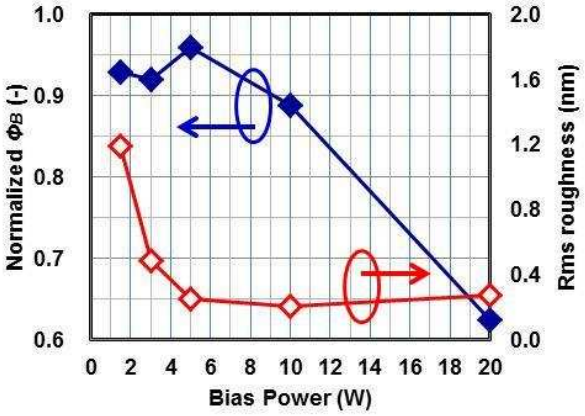

Fig. 2 Dependence of normalized ϕ_B, calculated from C-V measurements, and RMS roughness on bias power for BCl_3 etching.

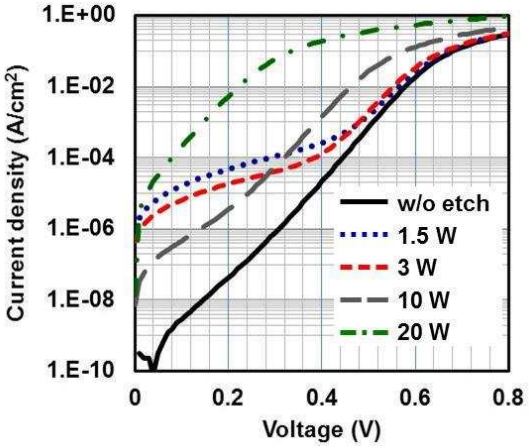

Fig. 3 Current-voltage characteristics of SBDs fabricated on the BCl_2 etched surface.

2) Cl_2/BCl_3 etching

Figure 4 shows the AFM images of GaN surface etched by the Cl_2/BCl_3 etching process. Figure 5 shows the dependence of RMS roughness on the bias power, and the comparison is plotted for BCl_3 and Cl_2/BCl_3 etching process. These results show that Cl_2/BCl_3 etching can realize a smooth etched surface even for a low bias, for example, at 2 W. It is believed that the amount of solid state compounds formed in the Cl_2/BCl_3 mixture is lower than that in pure BCl_3. Hence, a smooth surface can be realized under a low bias condition.

As shown in Fig. 6, low bias power Cl_2/BCl_3 etching processes achieved extremely low degradation of ϕ_B. Moreover, I-V curves obtained at low bias conditions (2 - 10 W) did not exhibit any plateau-like current leakage characteristics (Fig. 7). These results suggested that low bias power Cl_2/BCl_3 etching enable the realization of low damage recess etching.

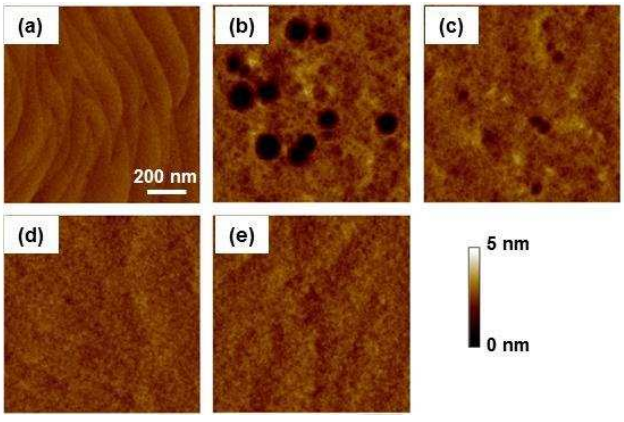

Fig. 4 AFM images of Cl_2/BCl_3 etched GaN surface; (a)as-grown, (b)bias power 1.5 W, (c)bias power 2 W, (d)bias power 5 W, (e)bias power 10 W.

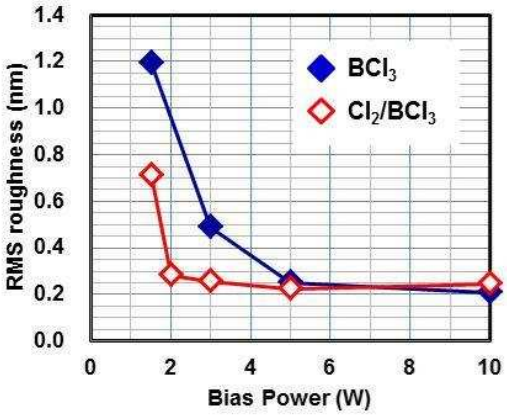

Fig. 5 Comparison of RMS roughness obtained from BCl_3 and Cl_2/BCl_3 etching.

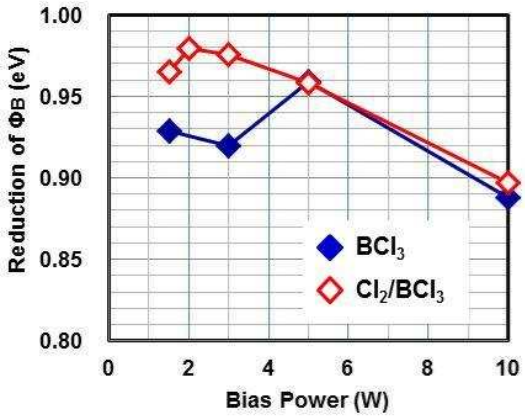

Fig. 6 Comparison of normalized ϕ_B obtained from C-V measurements for BCl_3 and Cl_2/BCl_3 etching.

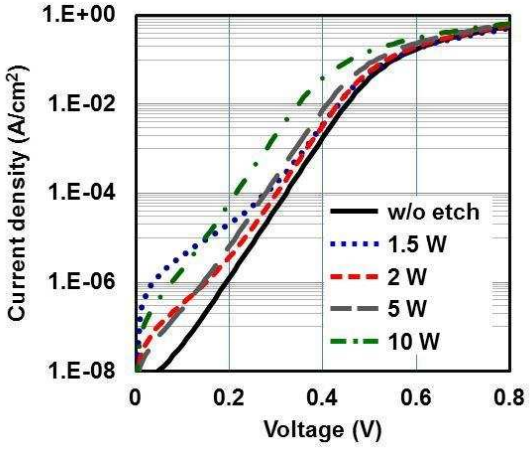

Fig. 7 Current-voltage characteristics of SBDs fabricated on the Cl_2/BCl_3 etched surface.

3) Applications to fabricating recess gate AlGaN/GaN-HEMTs

Low bias power Cl_2/BCl_3 etching was employed to fabricate recess gate AlGaN/GaN-HEMTs. Figure 8 shows the schematic of the device structures fabricated in this study. Devices were fabricated on two different epitaxial structures: a conventional structure (Fig.8(a)) and one with a thick AlGaN layer (Fig.8(b)). Cl_2/BCl_3 etching with a low etching power (2 W) was applied to the device with the thick AlGaN structure (Fig.8(c)). The etching depth was controlled so that AlGaN thickness after etching was nearly equal to the conventional AlGaN thickness. All devices were passivated with PECVD SiN.

The transfer characteristics for the AlGaN/GaN-HEMTs (L_g = 0.65 μm) were measured at V_d = 10 V. As shown in Fig. 9, the thick AlGaN layer with recess gate structure could have possibly caused the increase drain current and maximum transconductance as compared to those obtained with a conventional structure. However, note that there was almost no difference in the threshold voltage, as can be seen in Fig. 9. These improvements resulted from the low sheet resistance of the thick AlGaN structure and low damage recess etching.

Figure 10 shows pulsed I-V curves of fabricated AlGaN/GaN-HEMTs (L_g = 0.65 μm). V_{gs} was stepped from -3 V to +2 V with a 0.5 V step. For evaluating current collapse, bias stress was V_{gs} = -3 V and V_{ds} = 50 V. The pulsed I-V curves show that the gate recess structure resulted in an increased drain current of 700 A/mm as compared with a drain current of 600 A/mm obtain for the conventional HEMT. Moreover, current collapse ratio defined (I_d at V_d = 5 V with bias stress / I_d at V_d = 5 V without stress) for the gate recess structure and conventional structure were 89.5% and 81.0%, respectively. These results suggested that the etching damage caused by low power etching had negligible effect on device operation.

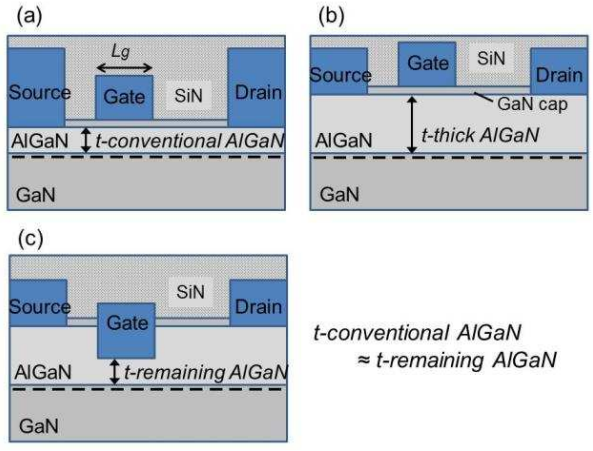

Fig. 8 Schematic of fabricated AlGaN/GaN-HEMTs; (a) conventional, (b) thick AlGaN epitaxial layer, (c) gate recess structure.

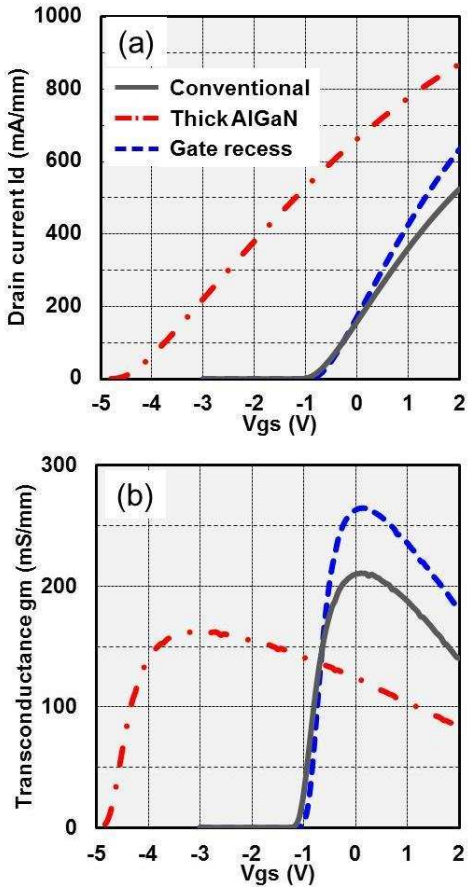

Fig. 9 Transfer characteristics of fabricated AlGaN/GaN-HEMTs; (a)I_d-V_{gs} curves, (b)transconductances.

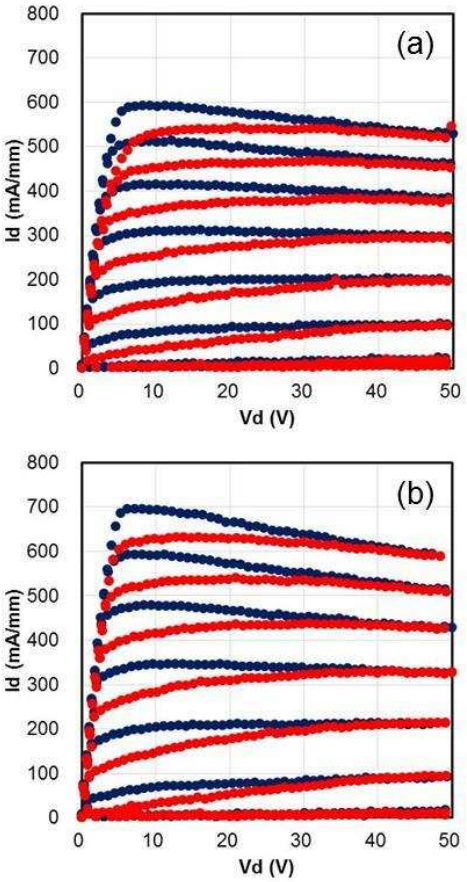

Fig. 10 Pulsed I-V curves of fabricated AlGaN/GaN-HEMTs; (a)conventional, (b) gate recess structure. V_{gs} was stepped from -3 V to +2 V with a 0.5 V step. The bias stress was V_{gs} = -3 V and V_{ds} = 50 V.

CONCLUSIONS

The authors reported on low damage etching of GaN using a low bias power. The results of AFM measurements and C-V measurements of the etched GaN surface indicated that a highly smooth surface and an extremely low degradation of ϕ_B were realized by BCl_3/Cl_2 etching with low bias power (e.g. 2 W). The optimized low power etching employed to fabricate recess gate AlGaN/GaN-HEMTs. The results revealed that excellent device performance could be realized with low power BCl_3/Cl_2 etching process.

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ACRONYMS

HEMT: High Electron Mobility Transistor
SBD: Schottky Barrier Diode
ICP: Inductively Coupled Plasma
MOCVD: Metal Organic Chemical Vapor Deposition
AFM: Atomic Force Microscopy
RMS: Root Mean Square
PECVD: Plasma-Enhanced Chemical Vapor Deposition