A Low-Annealing-Temperature Process Using Si-Incorporated Contact Stacks for n-Type III-Nitride Semiconductors

Yi-Che Lee, A F M Saniul Haq and Shyh-Chiang Shen*

School of Electrical and Computer Engineering, Georgia Institute of Technology,
777 Atlantic Drive NW, Atlanta, GA 30332-0250
*Email: shensc@ece.gatech.edu; Tel: 404-894-1884

Keywords: III-Nitride, n-type, ohmic contact.

Abstract

We report a metal contact scheme for n-type III-nitride (III-N) semiconductors using silicon-incorporated metal stacks. The use of silicon as the first layer of the deposition allows for improved ohmic contact resistance at low post-deposition annealing temperature. When implementing such metal stacks on an AlGaN/GaN heterojunction field-effect transistor structure, the specific contact resistance of 3.7E-6 Ω·cm^2 for the Si/Al-based contact with an annealing temperature of 675^{o}C. The surface roughness of 50.1 nm was also measured in the annealed drain and the source contact regions. The results suggest that the incorporation of a thin silicon layer in typical Ti/Al-based n-type III-N ohmic contact formation schemes help achieve smoother post-annealing surface roughness with a reduction in the annealing temperature.

INTRODUCTION

III-Nitride (III-N) semiconductors have become widely accepted materials systems for a wide variety of optoelectronic and electronic applications. The formation of the ohmic contact properties for III-N devices plays crucial parts in the multitude of the device performance. For examples, III-N heterojunction field-effect transistors (HFETs) have demonstrated high current drive and high frequency operation owing to their high carrier density and high electron mobility properties. Although the channel mobility is high which leads to much improved on-state resistance, the series resistance arising from the ohmic contact limits the ultimate switching loss achievable in III-N-based power electronics. There is a need for optimized contact schemes for the minimized drain and source contact resistance for III-N HFETs.

To form an n-type ohmic contact, the contacting materials would preferably have a work function shallower than that for the n-type semiconductor. In the case of GaN, the electron affinity is 4.11 eV [1] and contacting materials with the work function shallower than this value are of interests. Several studies on the n-type ohmic contact have been investigated in III-N materials [2-3]. Usually, ohmic contact on the n-type III-N can be achieved using Ti/Al-based metal stacks such as Ti/Al/Ni/Au, Ti/Al/Mo/Au and Ti/Al/Ti/Au [4-7]. In such multi-layer ohmic contact schemes, the formation of the interfacial TiN, $AlTi_2N$, along with a transitional Ti_3Al layer, facilitate low work function layer for the wide-bandgap materials. Luther et. al. concluded that the formation of TiN (with a work function of 3.74 eV) at the metal-semiconductor interface is essential for creating the ohmic contact [8-9]. In these ohmic contact formation, post-deposition annealing steps are usually required and the annealing temperature is usually high (>750^{o}C). Although they enabled low-resistance contact, the surface morphology was usually rough that may limit the practical use of these schemes [3]. Approaches to achieve smooth surface morphology along with low contact resistance in the drain and the source region were actively sought. For examples, heavily-doped contact region can be used to form low-resistance drain/source pads, which requires complex re-growth epitaxial processes or ion-implantation [10-11]. Other studies on Al-containing metal stacks for n-GaN ohmic contacts were also studied, such as the use of Pd/Al [12], Ta/Al [13], Hf/Al [14], or Nd/Al [15].

In this paper, we report a study on the improved ohmic contact property for n-type III-N using e-beam evaporated silicon-aluminum (Si/Al)-based stacks. Si was chosen as a choice for the contact material for its shallow work function of ~4.1 eV [16]. Our study shows that the proposed Si-incorporated metal stack could achieve a low specific contact resistance of 3.7E-6 Ω·cm^2 and a surface roughness of 50.1 nm when an AlGaN/GaN HFET sample was annealed at a temperature of 675 ^{o}C. The XPS results also shows that the silicon is diffused into the GaN layers, which may also contribute to the further reduction of the contact resistance in the drain and the source region. Our results suggested that the incorporation of a thin Si film in the n-type III-N ohmic contact stacks may provide an alternative approach to achieving low-resistance contact region at a low annealing temperature.

EXPERIMENTS

The ohmic contact experiments were performed using an $Al_{0.25}Ga_{0.75}N$/AlN/GaN HFET epitaxial samples grown on a p-type silicon substrate. The epitaxial layers consist of a few

microns of GaN buffer layer, 1.5 microns of undoped GaN layer, a 1-nm AlN binary barrier layer, a 30-nm $Al_{0.25}Ga_{0.75}N$ barrier layer and a 1-nm GaN cap layer. The fabrication processing starts with an isolation mesa etching using a low-damage inductively coupled plasma (ICP) process. The metal contact pad patterns with a pad size of 20µm×80µm were then deposited using an e-beam evaporator for the transmission line method (TLM) patterns. The adjacent TLM metal contact pads have a spacing of 2µm, 4µm, 8µm, 16µm, and 32µm, respectively, in a set of the TLM. In this study, two metal stack, one with Si/Al/Ti/Au =100/500/250/500Å and the other one with Si/Al/Ti/Au = 125/500/250/500Å were deposited on the AlGaN/GaN HFET samples to explore the impact of the annealing conditions on the resulting contact resistance and the surface morphology. Preliminary studies showed that although higher annealing temperature may provide low contact resistance, these conditions led to a rough surface after the post-deposition annealing, which is not of interest for the purpose of the study. Consequently, three annealing temperatures (675 °C, 700 °C and 725 °C) and three annealing time (2.5, 5, and 10 minutes) were chosen for the annealing study for the two metal stacks (18 samples total) in this study set. For comparison, we also prepare samples with a typical Ti/Al/Ti/Au n-type contact on the same HFET structure and were annealed at 750 °C for the study.

The specific sheet resistance and the specific contact resistance were evaluated using a rectangular TLM patterns as described in the previous paragraph using Keithly 4200-SCS semiconductor parameter analyzer. Four-point probe methods were applied for the resistance measurement to exclude the series resistance arising from the contact probes. At least three sets of TLM measurements were performed in each of the 18 samples.

Results and Discussions

Table I summarizes the contact resistance measured with the proposed Si/Al-based metal stack from the TLM measurement. The fitting linearity was >0.999 for each measured data point. The low temperature and longer anneal time for post-deposition annealing indicates that the Si/Al/Ti/Au stacks require proper thermal energy for silicon diffusion and ohmic contact formation.

TABLE I. A Summary chart showing the contact resistance measurement results using Si/Al/Ti/Au metal layers

Metal layer Thickness		Specific contact resistance, $\rho_{c,sp}$ ($\Omega \cdot cm^2$)		
	Temp. (˚C)	Time = 2.5 min	Time = 5 min	Time = 10 min
Si/Al/Ti/Au = 100/500/250/500Å	675	2.4E-5	7.6E-6	3.8E-6
	700	1.8E-5	6.4E-6	8.4E-6
	725	9.2E-6	5.7E-6	7.1E-5
Si/Al/Ti/Au = 125/500/250/500Å	675	2.0E-5	5.0E-6	3.7E-6
	700	4.8E-6	8.8E-6	8.6E-6
	725	4.1E-6	9.1E-6	1.3E-5

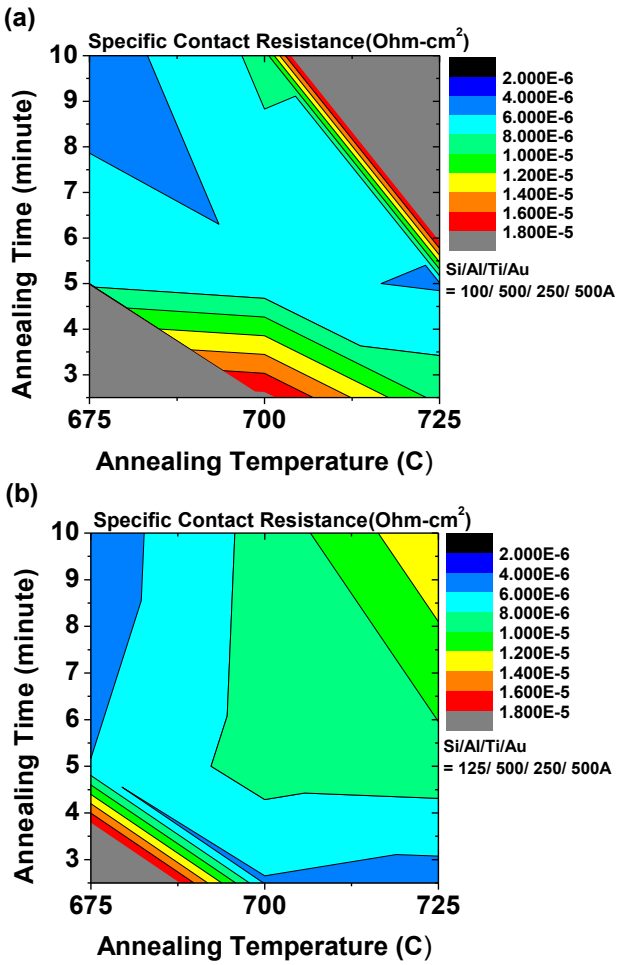


Figure 1. The contour plots of specific contact resistance of (a) 100 A Si and (b) 125 A Si layer of Si/Al/Ti/Au stacks with different annealing time and temperature on AlGaN/AlN/GaN HFET samples.

Shown in Fig. 1 are the contour plots of the measured specific contact resistance versus the annealing time and the temperature for the two Si/Al/Ti/Au stacks under study. In both plots, the lowest specific contact resistance can be consistently achieved with longer annealing time at annealing temperature of 675 °C. For samples with 125-Å-thick Si layer, the low-resistance could be achieved with the annealing time greater than 5 minute and similar contact properties may be achieved at temperature > 700 °C at a relatively short sintering time. The data shows that the sample with 125-Å-thick Si layer may have a wider processing window than those with 100-Å Si layer.

Table II shows a comparison of the Si/Al-based ohmic contact annealed at 675 °C and a Ti/Al-based contact annealed at 750 °C for the same HFET structure. Both Si/Al/Ti/Au stacks achieved a contact resistance < 4E-6 Ω-cm^2 at the annealing temperature at 675 ˚C, while the n-type contact using "conventional" Ti/Al/Ti/Au metal systems shows a much higher contact resistance at 750 ˚C. The data

demonstrated the advantages of using Si/Al-based material stacks for low-temperature annealing process.

TABLE II. THE SUMMARY OF SI/AL/TI/AU AND TI/AL/TI/AU OHMIC CONTACTS

	Anneal. Temp. (˚C)	$\rho_{c,sp}$ ($\Omega\cdot cm^2$)	$R_{C,sp}$ ($\Omega\cdot mm$)
Si/Al/Ti/Au (125/500/250/500Å)	675	3.7E-06	0.32
Si/Al/Ti/Au (100/500/250/500Å)	675	3.8E-6	0.33
Ti/Al/Ti/Au (300/700/300/500Å)	750	8E-06	0.46

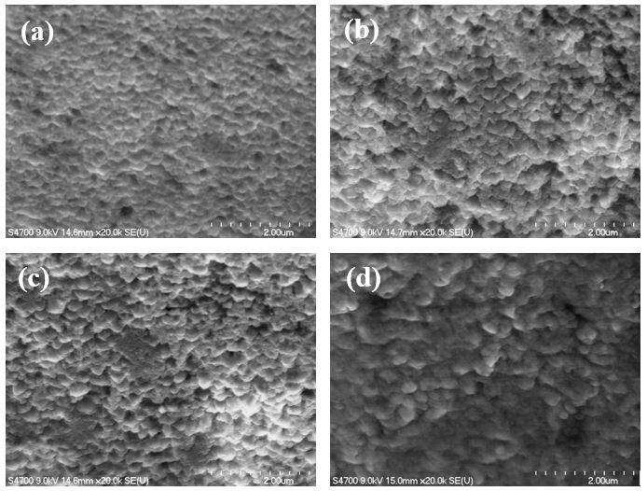
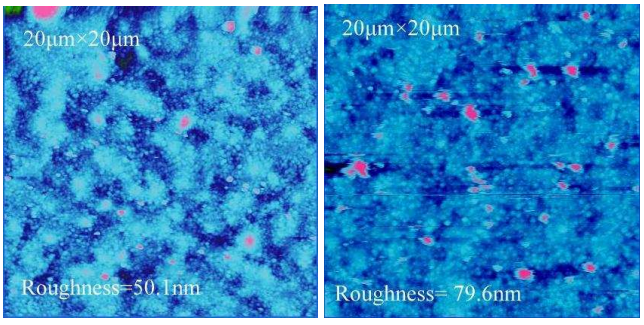


Figure 2. SEM pictures of Si/Al-based stacks after post-deposition annealing for 5minutes at (a) 675 ˚C, (b) 700 ˚C, (c) 725 ˚C, respectively. (d) a SEM picture of and Ti/Al-based metal annealed at 750 ˚C for 5 minutes for a comparison.

Shown in Fig. 2 are SEM pictures of Si/Al-based contacts annealed at different conditions. The picture indicates that the roughness increases with an increase in the annealing temperature from 675 ^{o}C to 725 ^{o}C. For a reference, an SEM of the post-annealing metal surface of the Ti/Al-based contact (annealed at 750 ^{o}C) is also shown for comparison (Fig. 2(d)). The rough texture in the annealed contact region may results in non-uniform resistance distribution in the metal pads. With a reduced annealing temperature, smoother surface can be achieved for Si/Al-based stacks.



(a) (b)

Figure 3: AFM scan of 125 A thick Si-based metal stack for (a) 675C 5min, and (b) 700C 5min post-deposition annealing.

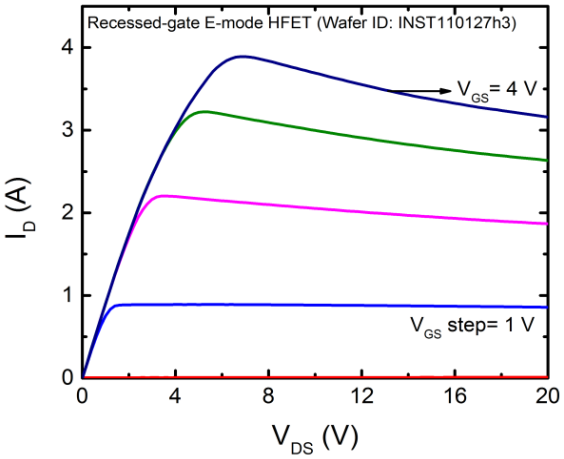


Figure 4. I_D-V_{DS} family curve of 10-mm wide recessed-gate E-mode HFET.

The surface roughness of the annealed Si/Al-based metal stacks was also measured by a Veeco atomic-force microscopy (AFM) system. As shown in Fig. 3, the results were obtained from the 20μm×20μm AFM scans in the post-annealing contact area of the Si/Al/Ti/Au stack with 125-Å-thick Si layer. The root-mean-square (RMS) surface roughness is 50.1nm and 79.6nm for the annealing temperatures of 675 ˚C and 700 ˚C for 5 minutes, respectively. In comparison, the roughness of the Ti/Al/Ti/Au contact annealed at 750 ˚C for 5 minutes shows an RMS value of 82.6 nm (not shown here). In a further study using an x-ray photoelectron spectroscopy (XPS)-based depth profile, we observed that silicon is diffused into the underlying AlGaN and GaN layer in the contact and the nitrogen being out-diffused into the metal layer, creating significant intermixing of the contact after the post-deposition annealing. It is concluded that the incorporation of silicon in the contact stacks with lowered annealing temperature not only helps improve the contact resistance but also provides the flexibility of the process integration for III-N device fabrication by offering a much lower thermal budget in the ohmic contact formation, with an added benefit of achieving smooth post-annealing metal surface.

Shown in Figure 4 is a I-V family curves of a recessed-gate AlGaN/AlN/GaN HFETs fabricated with the Si/Al/Ti/Au drain/source contacts. The recessed-gate structure was fabricated using an electrode-less photochemical etch-stop and a remote oxygen plasma oxidation technique reported previously in [17-18]. The devices were passivated using a benzocyclobutene (BCB) layer before the Metal 1 deposition. The device has a gate width of 10 mm (0.5mm × 20-fingers) with L_{GS} = 13.5 μm and L_G = 3.5 μm. The threshold voltage (V_{th}) was V_{th} = 0.08 V determined at I_{DS} = 1 mA/mm. The $I_{D,max}$ of 3.9A was achieved (390 mA/mm) was measured at V_{GS} = 4 V. For a comparison, the I_{Dmax} for a single-finger unit-cell device

9

showed I_{Dmax} = 420 mA/mm. The results suggest uniform current distribution was achieved across the 20-finger device. The on-state resistance ($R_{on} \cdot A$) was estimated to be 10.89 Ω-mm and the specific contact resistance was 5.2e-6 Ω-cm^2 with a transfer length of 1.8 μm for the completed wafer piece.

CONCLUSIONS

In summary, we report an n-type III-N ohmic contact using Si/Al/Ti/Au material stack in a single-pass e-beam evaporation. The lowered post-deposition annealing temperature may result in better ohmic contact surface morphology that may provide the flexibility for further process integration of III-N device including but not limited to AlGaN/GaN HFETs.

ACKNOWLEDGEMENTS

The authors would like to thank the support of the staffs of IEN, Georgia Institute of Technology, for their support during the processing and data acquisition and partial financial support by Intersil Corp., CA.

REFERENCES

[1] Maeda Masakatsu, Yamasaki Takao, Takahashi Yasuo, "Ohmic Contact Mechanism of Titanium-based electrodes on n-type Gallium Nitride," in Transaction JWRI, vol. 41, no. 1, 2012.

[2] J-C. Gerbedoen, A. Soltani, M. Mattalah, A. Telia, D. Troadec, B. Abdallah, E. Gautron, J-C. De Jaeger, "Study of Ohmic Contact Formation on AlGaN/GaN HEMT with AlN spacer on Silicon Substrate," in the Proc. 4th Europn Microwave Integrated Circuits Conf., pp. 136, Rome, Italy, 2009.

[3] Fitih M. Mohammed, Liang Wang, Ilesanmi Adesida, and Eddie Piner, "The role of barrier layer on Ohmic performance of Ti ⁄ Al -based contact metallizations on AlGaN ⁄ GaN heterostructures" J. of Appl. Phys. 100, 023708, 2006

[4] S. Ruvimov, Z. Liliental-Weber, J. Washburn, K. J. Duxstad, E. E. Haller, Z.-F. Fan, S. N. Mohammad, W. Kim, A. E. Botchkarev, and H. Morkoc¸, "Microstructure of Ti/Al and Ti/Al/Ni/Au Ohmic contacts for n-GaN" Appl. Phys. Lett. 69, 1556, 1996.

[5] Z.-F. Fan, S. N. Mohammad, W. Kim, O. Aktas, A. E. Botchkarev, and H. Morkoc¸, "Very low resistance multilayer Ohmic contact to n-GaN" Appl. Phys. Lett. 68, 1672, 1996.

[6] S.J. Cai, R. Li, Y.L. Chen, L. Wong, W.G. Wu, S.G. Thomas and K.L. Wang," High performance AIGaN/GaN HEMT with improved Ohmic contacts," in Electron. Lett. vol. 34, No. 24, 1998.

[7] A. Motayed, R. Bathe, M. C. Wood, O. S. Diouf, R. D. Vispute, S. N. Mohammad, "Electrical, thermal, and microstructural characteristics of Ti/AlTi/Au multilayer Ohmic contacts to n-type GaN," J. Appl. Phys. vol. 93, No. 2, 2003

[8] B P Luther, S E Mohney, and T N Jackson, "Titanium and titanium nitride contacts to n-type gallium nitride," in Semicond. Sci. Technol. **13**, 1322-1327, 1998.

[9] V. Rajagopal Reddy, C. K. Ramesh, "Low-resistance ohmic contacts to n-type GaN using Ti/Al/Re/Au multilayer scheme," in Journal of Optoelectronics and Advanced Materials Vol. 6, No. 1, p. 177 – 182, 2004.

[10] S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, "Mass transport regrowth of GaN for ohmic contacts to AlGaN/GaN," Appl. Phys. Lett., vol. 78, pp. 2876, 2001.

[11] H.-C. Seo, P. Chapman, H.-I. Cho, J.-H. Lee, and K. Kim," Ti-based non-alloyed Ohmic contacts for $Al_{0.15}Ga_{0.85}N$⁄ GaN high electron mobility transistors using regrown n^+-GaN by plasma assisted molecular beam epitaxy," App. Phys. Lett., vol. 93, pp.102102, 2008.

[12] A. T. Ping, M. Asif Khan, and I. Adesida, "Ohmic Contacts to n-Type GaN Using Pd/AI Metallization," J. Electron. Mater. 25, 819, 1996.

[13] B. P. Luther, S. E. Mohney, J. M. DeLucca, and R. F. Karlicek, "Study of Contact Resistivity, Mechanical Integrity, and Thermal Stability of Ti/AI and Ta/AI Ohmic Contacts to n-Type GaN," Journal of Electronic Materials, vol. 27, No. 4, 1998.

[14] Norimasa Yafune, Motoi Nagamori, Hironari Chikaoka, Fuminao Watanabe, Keiichi Sakuno, and Masaaki Kuzuhara, "Low-Resistivity V/Al/Mo/Au Ohmic Contacts on AlGaN/GaN Annealed at Low Temperatures," Japanese Journal of Applied Physics 49, 04DF10, 2010.

[15] C. T. Lee, M. Y. Yeh, and Y. T. Lyu, J. Electron. Mater. 26, 262, 1997.

[16] http://www.el-cat.com/silicon-properties.htm

[17] Yi-Che Lee, Tsung-Ting Kao, J. Merola and Shyh-Chiang Shen, "A Remote-Oxygen-Plasma Surface Treatment Technique for III-Nitride Heterojunction Field-Effect Transistors," in IEEE Trans. Electron Dev., vol. 61, no. 2, 2014.

[18] Yi-Che Lee, Tsung-Ting Kao and Shyh-Chiang Shen, "A Study on Al_2O_3 Deposition by Atomic Layer Deposition for III-Nitride Metal-Insulator-Semiconductor Field Effect Transistors," in Dig. Of the 2013 CSMANTECH Conference, New Orleans, Louisiana, USA, 2013.

ACRONYMS

AFM: Atomic Force Microscopy
ALD: Atomic Layer Deposition
BCB: benzocyclobutene
III-N: III-Nitride
HFET: Heterojunction Field-Effect Transistor
TLM: Transmission Line Model
SEM: Scanning Electron Microscopy
XPS: X-ray Photoelectron Spectroscopy