Impact of Post Fabrication Annealing PEALD ZrO_2 for GaN MOSFETs

K. Bothe[1], A. Ma[1], A. Afshar[2], P. Motamedi[2], K. Cadien[2] and D. Barlage[1]

[1]Department of Electrical and Computer Engineering, University of Alberta, Edmonton, Canada
[2]Department of Chemical and Material Engineering, University of Alberta, Edmonton, Canada
kbothe@ualberta.ca

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Abstract

In this paper we examined the thermal stability of ZrO_2 gate dielectrics in GaN MOSFETs. The ultra-thin films were grown by low temperature plasma-enhanced atomic layer deposition (PEALD). It was determined that the high-k films required activation temperatures in excess of 400°C. This reduced the density of interface traps below ~10^{11} $eV^{-1}cm^{-2}$ and improved the device characteristics. The 500°C annealed ZrO_2 demonstrated an increased drain current density of 5x over the non-annealed ZrO_2 gate dielectric. However, annealing temperatures excess of 500°C severely degraded the Cr/ZrO_2/GaN interface and device. Likewise, Ti and Hf gate metals were unable to prevent degradation beyond 300°C and 400°C, respectively. The improved gate dielectric/GaN interface was achieved through the combination of a low temperature high-κ deposition technique followed by a post fabrication anneal.

INTRODUCTION

Low temperature plasma-enhanced atomic layer deposition (PEALD) gate dielectrics have demonstrated improved characteristics for GaN MOS structures. The MOS channel architecture has the potential for improved power devices because of the inherent off-state and enhancement-mode behavior [1]. Furthermore, the MOS architecture has the advantage of a reduced leakage current and gate length scalability over heterojunction field effect transistors (HFETs) [2-6]. Over the past few years, dielectric/GaN characteristics have significantly improved with the use of ultra-thin rare earth metal oxides [7]. The deposition technique has the most impact on the interface quality along the GaN channel. However, through post fabrication annealing the gate dielectric and dielectric/semiconductor interface can be improved to further reduce the interface traps along the channel. In this work, we present the post fabrication annealing effects of a GaN MOSFET with a PEALD ZrO_2 gate dielectric.

FABRICATION PROCESS

GaN MOSFET devices, shown in Figure 1, were fabricated on unintentionally doped GaN-on-sapphire templates. A 40 cycles ZrO_2 gate dielectric (~7 nm) was selectively deposited at 100°C via PEALD in a Kurt J. Lesker reactor at constant pressure of 1 Torr. The alternating precursor gases and corresponding dose/purge times were tetrakis(dimethylamido)-zirconium (0.04/5s) and oxygen plasma (2/2s). The low temperature deposition technique has demonstrated a reduced density of interface traps and a high capacitance density [8]. Furthermore, the deposited film was amorphous based on x-ray diffraction measurements; however, as the film was annealed the structure became polycrystalline [9].

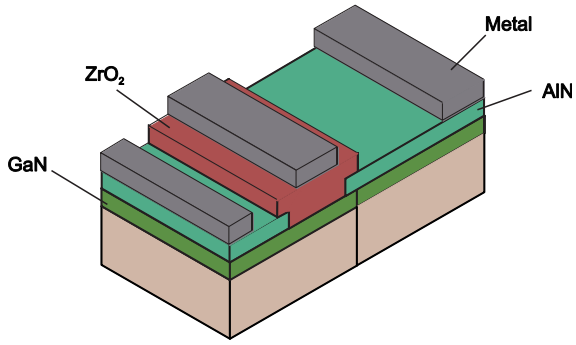

Figure 1: Device schematic of the GaN MOSFET with the low temperature PEALD ZrO_2 as the gate dielectric.

The source and drain regions were defined by ultra-thin PEALD AlN (~3 nm) films [10]. The selectively deposited low temperature AlN film was grown at 250°C with a constant pressure of 1 Torr. The 40 cycles of alternating precursor gases and corresponding dose/purge times were trimethyl-aluminum (0.02/7s) and nitrogen plasma (10/7s). The low temperature AlN films produced a moderate 2DEG density ($6.2x10^{12}$ cm^{-2}) along the AlN/GaN interface. Similar to other deposition techniques, the PEALD AlN interface charge density was dependent with film thickness [11].

Sputtered Cr/Au (20nm/80nm) was used to define the gate, source and drain contacts. Large 100x100µm GaN MOSFETs were used to characterize the effects of annealing the gate dielectric. The devices were exposed to the defined annealing temperature for 15 minutes in a nitrogen rich environment. Following the post fabrication annealing, electrical tests were performed to evaluate the transistors gate dielectric characteristics and overall device behavior.

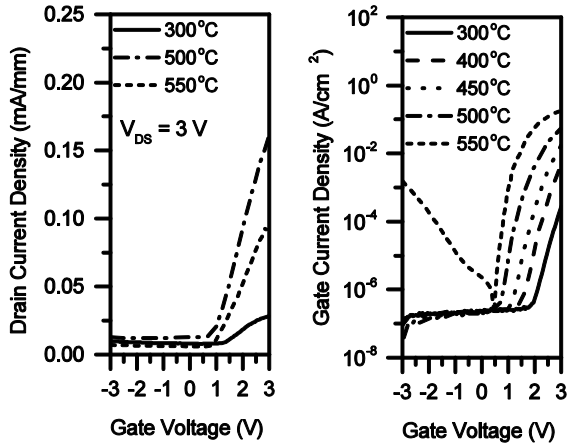

Figure 2: (a) Transfer characteristics of the GaN MOSFET with respect to post fabrication annelaing. (b) The corresponding gate leakage current based on device annealing.

EXPERIMENTAL RESULTS

Electrical measurements of the MOSFET were obtained after each annealing temperature to track the improvement and degradation of the gate dielectric. The GaN MOSFET exhibited enhancement-mode behavior with a threshold voltage of ~1V. The transfer characteristics, shown in Figure 2a, were examined as the gate dielectric was improved through temperature activation. The peak current density was increased up to an annealing temperature of 500°C through improvement of the gate dielectric and source and drain contacts. The tunneling contact resistance of the source and drain improved as the annealing temperature increased. However, beyond the optimal gate dielectric annealing temperature, the MOSFET was severally degraded as the current density was decreased. The reverse gate leakage current (Figure 2b) was a strong indication of when the gate dielectric and GaN interface was unable to withstand the annealing temperature. All annealing temperatures up to 500°C maintained a low reverse bias gate leakage current. However, beyond this temperature the gate leakage current increased, which indicated the addition of unwanted interface traps along the channel.

The annealing effects of the interface traps were examined through low frequency capacitance-voltage hysteresis [12] and conductance-frequency extractions [13]. The density of interface traps extracted from the frequency response, shown in Figure 3, was minimized at 500°C. This followed the transfer characteristics discussed earlier. As the ZrO_2 was exposed to 550°C annealing temperatures the density of interface traps increased by >10x. This was confirmed from the extracted D_{it} from the C-V hysteresis, shown in Table I. The annealing temperatures between 400°C and 500°C activated the dielectric without degrading the GaN interface. This maintained C-V hysteresis of ~11 mV which corresponded to interface traps ~5x10^{10} ev^{-1}cm^{-2}. At 550°C the hysteresis increased from 11mV to 208mV which followed the trend of the conductance frequency spectrum.

TABLE I
LOW FREQUENCY C-V HYSTERESIS AND CONTACT RESISTANCE

Annealing Temperature	Hysteresis (10 kHz)	Interface Traps ($eV^{-1}cm^{-2}$)	R_c (Ωcm^2)
No Anneal	23 mV	1.1x10^{11}	35
300°C	19 mV	9.2x10^{10}	13
400°C	11 mV	5.3x10^{10}	4.6
450°C	13 mV	6.4x10^{10}	3.8
500°C	11 mV	5.5x10^{10}	3.7
550°C	208 mV	9.9x10^{11}	2.9

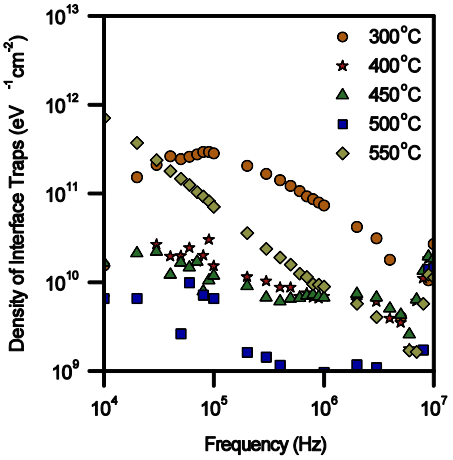

Figure 3: Density of interface traps (D_{it}) along the channel extracted from the conductance-frequency spectrum of the MOSFET.

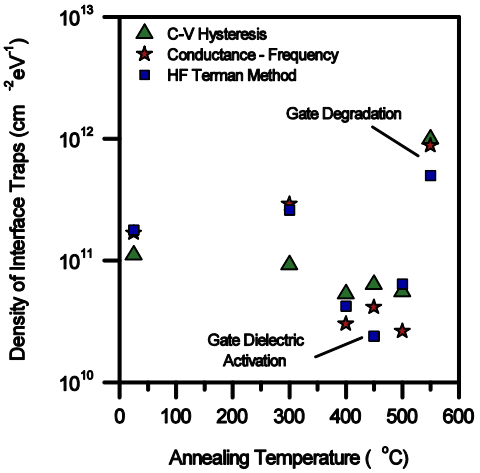

Figure 4: Extracted density of interface traps with respect to annealing temperature.

An optimal range for the gate dielectric was determined by comparing the density of interface traps with respect to the annealing temperature, shown in Figure 4. Annealing temperatures between 400°C and 500°C minimized the interface traps while activating the gate dielectric. Through various extraction techniques of the interface traps determined the optimal annealing regime to obtain improved ZrO_2 on GaN properties. The reduced contact resistance was minimal compared to the enhanced interface quality along the channel. Selective low temperature deposition of the gate dielectric followed by high temperature annealing was determined to improve the channel region of the enhancement-mode MOSFET with a Cr/ZrO_2/GaN stack.

To evaluate the effect of annealing temperature for different gate materials, metal oxide semiconductor capacitors (MOSCAP) were fabricated on the PEALD ZrO_2 films. The MOSCAPs structures were fabricated with the 40 cycles ZrO_2 recipe discussed earlier. The structures were patterned with different gate metals (Cr, Hf and Ti) where each material had a unique workfunction and melting point. The structures were annealed for 15 minutes at defined temperatures. The current-voltage and capacitance-frequency spectrums were used to evaluate the effects annealing temperatures had on the gate dielectric and channel interface.

The reverse bias gate leakage current of the MOSCAPs were examined before and after a 400°C post deposition anneal, shown in Figure 5. The leakage current of the Cr gate metal MOSCAP was unaffected after the 400°C anneal, whereas the Hf and Ti metals significantly increased by 10x and 200x, respectively. The interface traps (D_{it}) along the ZrO_2/GaN channel were extracted from the conductance-frequency spectrum during the depletion regime of the MOSCAP. The D_{it} followed the annealing effects of the leakage current after 400°C, shown in Figure 6. The Cr metal was able to maintain a low density of interface traps

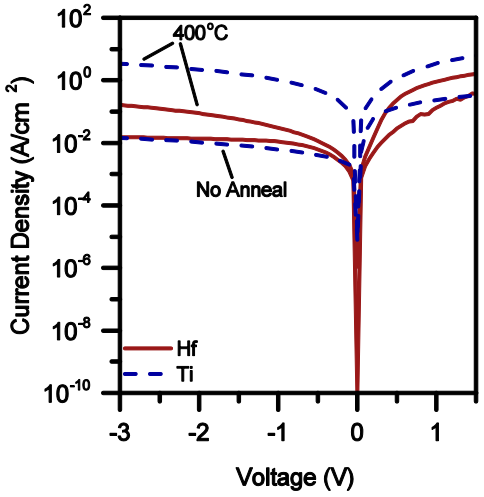

Figure 5: Temperature effects of the MOSCAPs gate dielectric leakage current with different gate metal. The Ti gate metal diffused more rapidly to cause higher reverse gate leakge current at 400°C.

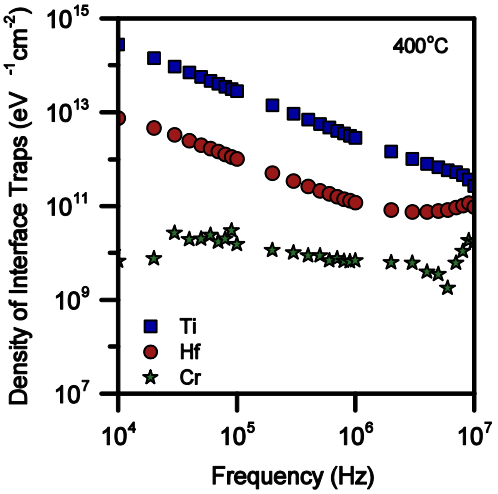

Figure 6: Extracrted density of interface traps (D_{it}) along the channel of the MOSCAPs at 400°C.

(< 10^{11} $eV^{-1}cm^{-2}$), compared to the Hf (~ 10^{12} $eV^{-1}cm^{-2}$) and Ti (~ 10^{13} - 10^{14} $eV^{-1}cm^{-2}$). This implied that the gate leakage current and density of interface traps were strongly dependent on the diffusion rate of the gate metal through the PEALD film. The maximum annealing temperature of the gate metals, shown in Table II, included minimum D_{it} obtained from the G_p-f spectrum and the melting point of the respective gate metal.

Based on the melting point of the metals, the Hf metal was expected to handle the highest temperature; however, the annealing induced density of interface traps prevented the maximum temperature from exceeding 400°C. We believe the optimal annealing temperature is dependent on the gate metal melting point, but more importantly on the overall phonon scattering effect of the ultrathin MOS stack. The incorporation of a thermally stable metal that is capable of reducing the MOS phonon scattering will potentially improve the maximum MOS annealing temperature and minimize the density of interface traps.

TABLE II
MOSCAPS GATE METAL CHARACTERISTICS

Gate Metal	Annealing Temperature	Minimum D_{it}	Melting Point
Cr	< 550°C	$5.3x10^{10}$	1907°C
Hf	< 400°C	$7.2x10^{10}$	2233°C
Ti	< 300°C	$4.8x10^{11}$	1668°C

CONCLUSION

Low temperature PEALD ZrO_2 and AlN films were incorporated into a GaN MOSFET. The annealing effects of the ZrO_2 gate dielectric was examined up to 550°C. Between 400°C and 500°C the interface traps were minimized which improved the peak current density. It was determined that annealing the device above 500°C severely degraded the

MOS channel along with the MOSFET device characteristics. With this, we have demonstrated the advantage of the incorporation of low temperature deposition followed by post fabrication annealing to improve the gate dielectric interface in GaN MOSFETs.

Furthermore, the degradation of the MOS channel based on different gate metals after annealing was examined through the characterization of MOSCAPs. The density of interface traps was strongly dependent on the annealing temperature and gate metal. In addition, we demonstrated the maximum annealing temperature of the MOS stack was not solely dependent on the melting point of the gate metal. To ensure a thermally stable MOS stack, the study of the gate metal is essential for the advancement of GaN MOSFETs.

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ACRONYMS

2DEG: Two Dimensional Electron Gas
AlN: Aluminum Nitride
Cr: Chromium
D_{it}: Density of Interface Traps
GaN: Gallium Nitride
Hf: Hafnium
HFET: Heterojunction Field Effect Transistor
MOS: Metal Oxide Semiconductor
MOSCAP: Metal Oxide Semiconductor Capacitor
MOSFET: Metal Oxide Semiconductor Field Effect Transistor
PEALD: Plasma-Enhanced Atomic Layer Deposition
Ti: Titanium
ZrO_2: Zirconium Oxide