SESSION 10
TEST/YIELD

Chairs: Gene Kohara, Marubeni America Corporation
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As more and more dies are packed into a single wafer, driven by return on investment (ROI), fabs are pressured to improve their testing methods and yield assessment prior to packaging. This Test and Yield Session presents five papers on topics from maximizing ROI to optimizing test yield methodology. The first paper, by Qorvo, presents a model for Return on Invested Capital (ROIC), applying it to epi uniformity improvement and adaptive masks as a test case. Using their ROIC framework, the authors found that both projects gave adequate return on investment. In the second paper, authors from WIN Semiconductor proposes a convenient numerical metric for quantifying the relative effectiveness of membrane probe card cleaning pads. Results are presented for six different commonly available cleaning pad materials and surface textures. The third paper in this session, by Itron France, describes a new method for determining the threshold voltage of a field-effect transistor (FET), applicable to all devices for which mobility exhibits a power-law dependence on carrier concentration. The authors show that the extracted threshold voltage has a useful physical meaning, and they demonstrate their method for several types of normally-on PHEMT and gated Hall-effect devices. In the fourth paper, authors from Qorvo, focus on known-good die (KGD) test failures caused by gold bond-pad contamination. They describe an oxygen-based plasma etch process that can improve gold bond pad cleaning and reduce false failure rates in KGD testing. The pad cleaning technique has reduced first-pass failures by 10% and eliminated the cost of retesting. The fifth and final paper, from Avago Technologies, describes a new approach for characterization of MIM capacitor leakage current and ramp-to-breakdown voltage, for developmental processes. By adding taps into a circuit's capacitors, the authors are able to perform stress and breakdown testing on nearly 100,000 capacitors per wafer (over 25 cm2 of total capacitor area) in a short time. This permits characterization of capacitor defect levels down to less than 0.1%, a level not possible with conventional PCM test approaches.