SESSION 11
MANUFACTURING IMPROVMENTS

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GaAs technology has reached a pretty mature level where high-volume MMIC chips can be manufactured with high yield and short cycle-time. However, as the III-V technology continues to advance there are always new challenges for the manufacturing engineers to address. In this Manufacturing Improvements session we have 5 excellent papers solving problems across different technologies. The first paper is from HRL where they walk us through the root cause and solution for the annoying seam defects caused by the mismatch of chrome mask dimensions with stepping distance at exposure. The second paper explains how Skyworks optimized a tape liftoff tool and improved the metal-polyimide adhesion to reduce die defects. The third paper by Qorvo details the methodology they used to ensure that critical dimensions are measured efficiently and accurately across a wafer at important layers in a high-volume manufacturing environment. The fourth paper by Sumitomo Electric Industries gives us a detailed view into forming narrow gates to fabricate GaN HEMT devices with 100GHz fT by using an i-Line stepper. The final paper shows how Qorvo readies a new process technology for prime time and high yield with an example showing how methodical changes to epi wafers and processing interact and affect yield and device performance in a new HBT process.