

# SESSION 7

## GaN DRY ETCH

**Chairs: Jansen Uyeda, Northrop Grumman (AS)**  
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As Wide Band Gap (WBG) power devices continue to move into high volume manufacturing, there is a need to improve associated plasma etch processes to achieve required process throughputs and yields. The papers in this section discuss plasma etch improvements for both GaN and SiC devices. The first paper in the session by SAMCO Inc. describes process optimization of SiC trench etching for SiC MOSFET applications. Silicon carbide can be a challenging material to etch. This paper describes the effects of process recipe parameters on the etch performance (rates and selectivities) and final feature characteristics (feature shape and morphology). The second paper of this session by Fujitsu Laboratories Ltd. discusses the optimization of a low damage GaN plasma etch process for GaN HEMT applications. Gate recess etch processes for GaN devices require precise etch depth control, smooth etched surfaces and minimal degradation of device performance (damage). The group describes the use of a Schottky Diode structure to evaluate plasma induced damage over a range of process parameters. Through optimization of plasma process and chemistry, a low etch rate / low damage etch process space is demonstrated that is suitable for GaN HEMT fabrication. The next paper in this session from Qorvo describes work to improve the productivity of the SiC through wafer via etch process. Through a combination of etch mask and plasma etch process optimization, SiC vias with smooth sidewalls and reduced post etch residues are demonstrated. The fourth paper of the session from Global Communication Semiconductors, LLC describes the production qualification of a SiC backside via fabrication process. The paper discusses the challenges encountered during development of a manufacturable process flow as well as descriptions of various test methods developed to evaluate the performance of the finished via structure. The session closes with a collaborative paper from Ferdinand-Braun-Institut and LayTec AG. This work explores methods to reduce mechanical failure of SiC wafers during the through-wafer substrate via process. The impact of various process steps, including wafer bonding and plasma etching, on wafer stress was measured in-situ during the fabrication process flow with a novel in-line measurement technique. Process improvements were tested and are described with their corresponding wafer stress measurements.

