Wafer-Level Packages for RF GaN Technologies & On-Wafer Humidity Test

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Abstract

Wafer-level chip-scale packaging is currently seen as a key technology affording a breakdown into integration of complex RF Front End with cost saving and performance enhancement.

Within this work, two chips scale packaging (CSP) concepts have been investigated in terms of manufacturability and process integration. In addition, a new Highly Accelerated Stress Test (HAST) configuration suited for on-wafer humidity testing has been designed to allow fast development cycles. A test vehicle circuit is used with a RF pre matched power transistor for the humidity tests.

Introduction

Two basic concepts are followed up for wafer level packaging (WLP). Concept A (Fig. 1) applies a BCB and a glass passivation. The MMIC is fully encapsulated by a BCB and a top glass layer.

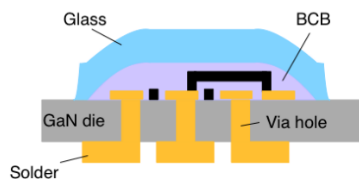


Fig. 1: Concept A – BCB & glass passivation

For the concept B (Fig. 2) an air-cavity package is realized using glass wafers having evaporated deposited glass walls that are joined to a GaN wafer by a bond process to achieve a hermetically closed chip-scale package. The electrical connection of the system is accomplished by a hot-via approach connecting signals and ground contacts from the backside of the wafer by through via-holes to the front side of the chip. An electroplated AuSn backside solder layer provides the interface to the system module. This approach suppresses the use of solder preforms.

The final hermitically sealed and small sized WLP MMIC product enables in both concepts the direct assembly on a PCB board without any additional packaging steps.

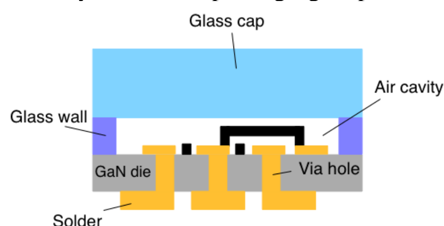


Fig. 2: Concept B – Hermetic air-cavity package

Both wafer level packaging approaches are based on the GH15 technology of UMS. This technology is a 150 nm gate GaN HEMT technology providing a power density of 4.0 W/mm for applications up to 35 GHz. Reference [1] shows additional information for both concepts.

Environmental reliability tests were carried out in order to show the evidence of a hermetical solution of concept A and B. The following paragraphs in this paper describes the test methodology and the results of humidity tests on WLP GaN test vehicles.

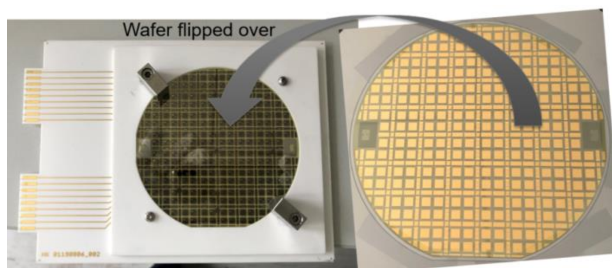
Environmental Humidity Tests

In this work an environmental test methodology is presented applying a novel on-wafer humidity test system. It enables short development cycles in the Front End wafer manufacturing area by achieving fast feedback loops of reliability results. The evaluation of technological process concepts can be done already in the very first development phases. In addition, it saves time and costs for chip assembly processes in test packages for humidity tests. As such, also side effects from a classical chip packaging manufacturing spread are not present, which therefore allows a better interpretation of the humidity test results. Especially for wafer-level chip-size packages, the on-wafer reliability system can be used for process qualification for instance.

The wafer-level humidity tests are carried out in an HAST test system. The test system allows a temperature range

from 105°C to 143°C at a relative humidity range from 75% to 100% in unsaturated operation. In dry and wet operation, the system enables the operation from 50°C to 95°C and from 50% RH to 95% RH. These applicable test conditions enables THB as well as HAST tests as specified in common standards [2]. Up to 72 cable feedthroughs enable the connection to an electrical test system for voltage biased tests.

Fig. 3 shows the test fixtures and the wafer test cards for the wafer biasing inside the chamber. Three wafer test cards have been manufactured in order to enable parallel wafer testing. The wafer test cards moved into individual slots of the cassette. The cassette comes with three plug-in card holders, which are wired to the feedthrough connectors inside the chamber. This configuration consists of 54 cable feedthroughs applied for connecting 6 DUT's (devices under test) per wafer at gate, drain and source.



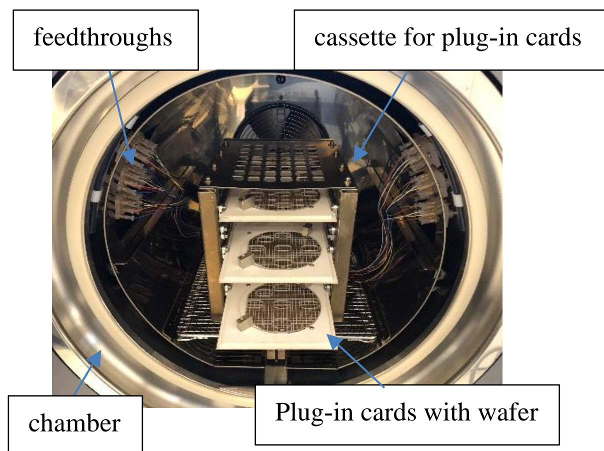


Fig. 3: On-wafer humidity test system setup

TEST CONDITIONS AND PROCEDURE

The wafer backside metal is used for the interconnection of the test vehicles on the wafer. A 1-mm gate width pre-matched transistor circuit is used. This design integrates active and passive elements and RF pads in ground-signal-ground (GSG) configuration. Through wafer via-holes are connecting the front side pads to the backside metallization of the wafer. The biasing of the devices is performed by needle that connects the plug-in card to the backside metal of the wafer.

Fig. 4 (top) shows the front side of the test vehicle. The Fig. 4 (bottom) depicts the contact pins locations on the backside of the test vehicle with the gate, source, and drain interconnections.

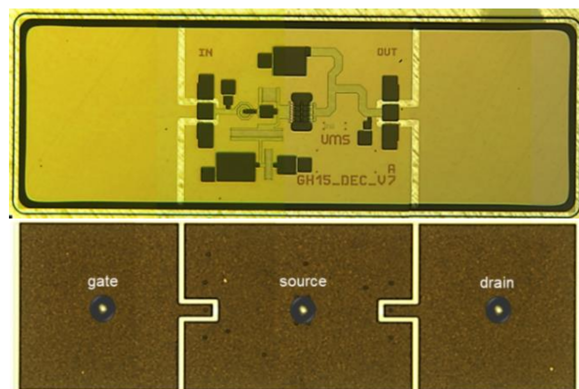


Fig. 4: Contact pin interconnection to test vehicle – test vehicle DEC (top); back side of test vehicle (bottom) & contact pin location from test card

After the wafer is mounted on the test card, a procedure is performed to manage a good electrical contact to each DUT's. In case of the GH15 technology the biasing conditions are Vg = -7 V for the gate voltage and Vd = +20V the drain voltage. As mentioned above, up to 18 DUT's can be biased and monitored on three wafers in parallel per test setup. Each DUT is biased separately before the test starts in order to identify any issue due to a poor electrical contact. After the contact test, a biased HTRB step is performed for 24 h at target temperature without humidity in order to sort electrical weak DUT's. Then all devices are again unbiased. After the humidity is switched on and the bias is applied again after the temperature and humidity reaches the target values. Test standards [2] specify HAST conditions with 130°C@85% RH associated to a criteria of 96 h test duration without any DUT failure. For THB conditions defined at 85°C@85% RH, the pass criteria is specified to get no failure within 1000h. Gate and drain currents are monitored by the electrical measurement system. In case of degradation of one device the electrical biasing stops at a current compliance of 2 mA. During THB test, interim visual inspections are done approximately every 300 h. In case of the HAST the test duration of >96 h will be performed without any interim inspection. Visual inspections of the DUT's are carried out before and after the test to identify any optical change for failed and passed devices.

TEST RESULTS OF WLP PROCESSED WAFER

In both evaluated WLP concepts the devices are packaged utilizing glass as final protection. A hermetic package solution is one major objective of the project. The

humidity tests should illustrate the need and correct integration of the glass for sufficient protection.

Concept A– BCB & glass passivation

Two wafers of concept A were mounted into the test chamber. One wafer is fully processed with BCB and glass and the other one without glass passivation. The motivation of this test configuration was to reveal the improved humidity protection of the glass in addition to the BCB passivation. Fig. 5 shows the failure plot of DUT's versus time tested with BCB & glass versus BCB only passivation. THB and HAST tests applied with a test duration of 1000 h and 150 h, respectively. Failures shown in the graph correspond to electrical sudden breakdown of the device in all the cases hitting the compliance at 2 mA gate or drain current. The humidity degradation of the device leads to a short of drain or gate to source. In case of the concept A the additional glass layer reduces drastically the failure rate in time. Two sudden failures of DUT occurred after re-start of interim inspection at around 667 h for the BCB & glass layer.

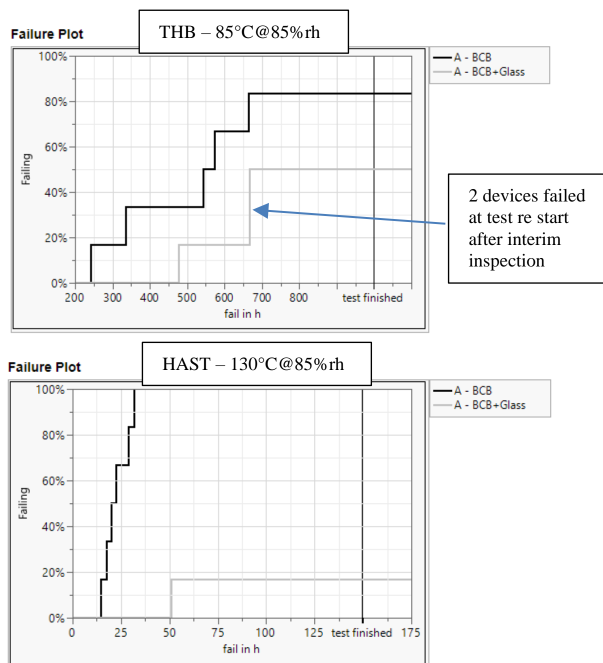


Fig. 5; Failure plot of THB (85°C@85% RH) in comparison of HAST (130°C@85% RH) of concept A

Optical inspection of all failed dies have shown one crack inside the glass and an electrical over stress (EOS) at the gate electrode (Fig. 6 a) for BCB & glass passivation. These failures are expected to have its root cause by uncontrolled change of glass layer stress and CTE mismatches of the passivation layers. Thermal cycling tests indicates a change of strain of the layers that lead to glass delamination. Consequently, the DUT reveals an electrical breakdown at the active device. In case of the BCB, the failed devices showed inside the active area a degradation of the semiconductor. This failure is identified typically as humidity related degradation in between the gate at -7V and drain area biased at +20V that result in a maximum applied voltage difference of 27 V. The mean failure rate of failed DUT's in case of the BCB passivated wafers for THB and HAST are in 471 h and 22.5 h, respectively. The degradation depicted in Fig. 6 b) occurs under HAST conditions 21 times faster compared to THB conditions.

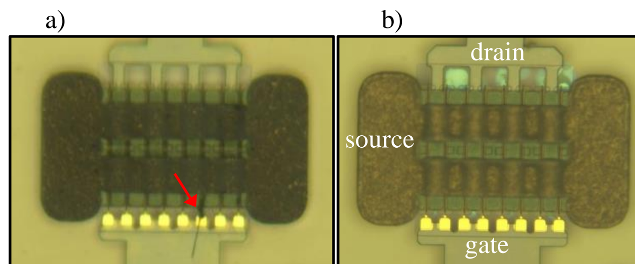


Fig. 6: Optical view of failed DUT's – a) BCB & glass (51 h) and b) BCB

Finally, the test shows a clear improvement of humidity protection by applying the glass passivation layer as expected. The reliability of the package A depends strongly on the mechanical strain control of the BCB and glass layer.

Concept B - Hermetic air cavity package

For concept B one wafer was tested in unbiased HAST conditions for 150 h. Unexpected process issues appeared due to layout reasons that made it impossible to finish the wafer at the backside process. The wafer was bonded to the glass cap wafer after completion of the front side process. Then the wafer was thinned down to a target thickness of 70 µm. The wafer manufacturing stopped after the grinding step. In order to investigate the humidity resistance of the air cavity package, the edge of the bonding interface had to be exposed first. A groove was sawed into the WLP wafer through the GaN on SiC Epi wafer up to the glass wafer allowing humidity penetration to the outer chip edges as shown in the SEM picture of Fig. 7 b).

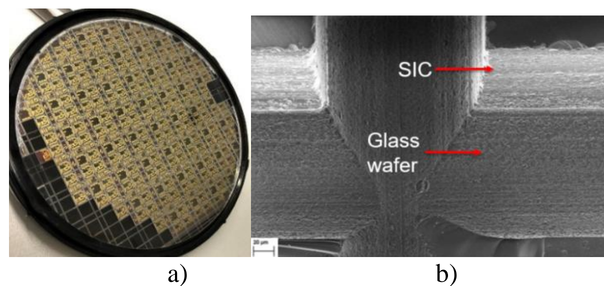


Fig. 7: a) WLP wafer after groove sawing – lower left part of wafer shows low bonding strength; b) tilt SEM view of groove with exposed bonding interface

The lower left part of the WLP wafer showed a small area with package yield loss after the sawing process. At this wafer area, a weak bonding interface could be identified as root cause (Fig. 7 a). After this preparation the WLP wafer was submitted to an unbiased HAST test for 150 h.

After 50 h and 100 h, an optical inspection was performed to evaluate any change or degradation of bonding interface by optical and mechanical characterization. Fig. 8 shows the top view of the test vehicle through the glass cap after 150 h unbiased HAST testing. No changes of the bond interfaces as well as no indications of humidity entrance into the air cavity have been detected by visual inspection.

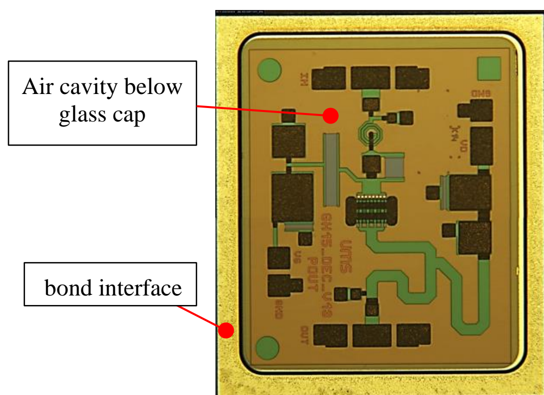


Fig. 8: top view of the test vehicle after 150h unbiased HAST exposure

Both wafer-level chip-scale packaging concepts had shown a clear step towards a hermetic packaging solution. The material glass supports this solution by its superior properties to stop moisture diffusion through the bulk.

Development Cycle

The application of on-wafer reliability tests enables a first and fast feedback about the process integration at the FE wafer manufacturing. On-wafer tests (OWT) should allow to reveal unexpected failures and to confirm the effectiveness of the process integration approach applied. However, it is important to apply representative tests taking into account the requirements for the technology processes. These requirements usually derived from final product specifications. Applying correct pass/fail criteria for on-wafer tests are mandatory prerequisites to sort the right variants for final product qualification in the right manner. Fig. 9 illustrates the flow diagram of the development cycle and the role of the OWT.

The on-wafer humidity test system in this work enables after completion of wafer manufacturing an HAST test result within around 15 days. The test in oven lasts around 6 days, 2 days for data analysis and additional 7 days for physical failure analysis if required.

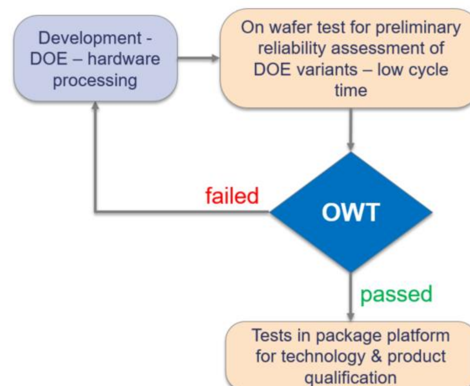


Fig. 9: Flow diagram for process development and testing

Conclusion

This work summarizes the implementation of an on-wafer humidity test system with the capability of DC biasing of test circuits. Two different WLP concepts were tested in this new designed OWT system using THB and HAST conditions in the frame of this work. The fast feedback loop and the objectives of on-wafer tests as well its results are extensively discussed.

Acknowledgements

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References

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Acronyms

CSP: Chip Scale Packaging
DUT: Device under Test
WLP: Wafer Level Packaging
CoGaN: Covered Galium Nitrid
THB: Temperature Humidity Bias
HAST: Highly Accelerated Stress Test
HTRB: High Temperature Reverse Bias
OWT: On Wafer Test