Analysis of GaN-HEMT DC-Characteristic Alterations by Gate Encapsulation Layer

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Abstract

In this paper, we investigate changes of DC characteristics in GaN HFETs linked to the intrinsic stress of the 2nd passivation layer (gate encapsulation). In the earlier work of our group, it was shown [1] that the leakage current of transistors is highly sensitive to the gate encapsulation with SiN_x. In this study, the device characteristics before and after encapsulation with 200 nm tensile/compressive SiN_x layer were analyzed. We show that a transferred strain underneath the gate contact caused by the intrinsic stress in SiN_x layer not only influences the reported leakage current but also changes threshold voltage (V_{th}) and maximum drain current (I_{DSmax}) of GaN HFETs. The obtained experimental results are consistent with the performed simulations.

INTRODUCTION

The influence of a stressed SiN_x passivation layer on GaN HFETs characteristics was reported in [1] and [2]. It is expected from theory that due to the piezoelectric nature of AlGaN/GaN epitaxial layers an external force applied to the gate structure leads to a local reduction/enhancement of the channel electron density and consequently tunes the device characteristic. In this work, the influence of intrinsic stress in the SiN_x passivation layer encapsulating the gate was investigated. For this purpose, we compared the DC characteristics of the same transistors before and after passivation with 200 nm nitride deposited in a PECVD system. Nitride layers with 1.5 GPa difference in intrinsic stress were compared. The investigations were additionally backed by physical device simulations optimized for predicting local strain variations.

EXPERIMENTAL

In this study, the transistors were fabricated on two identical 4 inch s.i. SiC substrates with MOVPE-grown epitaxial layers. The fabrication process includes the following steps: formation of ohmic contacts, deposition of 150 nm SiN_x as the first passivation layer, device isolation by multi-energy N^+ implantation, gates fabrication and DC characterization of the transistors. The first nitride layer was deposited using the same recipe for both test wafers. After the first set of measurements the gates were encapsulated with 200 nm SiN_x. For the wafer W1 a tensile recipe with + 0.5 GPa stressed nitride and for the wafer W2 a compressive recipe with about - 1.0 GPa intrinsic stress were used. The highly compressive intrinsic stress of SiN_x was realized by using a low frequency plasma excitation for the PECVD deposition process. Then the same transistors on both wafers have been characterized DC-wise. The electrical measurements were carried out on 2×50-µm transistors with 150 nm gate length, 0.5 µm source-gate and 1.5 µm drain-gate separation.

RESULTS AND DISCUSSION

Fig. 1 shows the mean-value output characteristics of 37 transistors measured before and after gate encapsulation. On wafer W1 with a tensile nitride (+ 0.5 GPa) as the second passivation, I_{DSmax} increased by about 0.15 A/mm, while on wafer W2 with the compressive nitride (- 1.0 GPa) the increase was only by 0.03 A/mm, as compared to the measurements before gate encapsulation. The increase in maximum current on wafer W1 indicates an enhancement of electron density in the 2DEG channel. Fig. 2 shows the wafer statistics of the threshold voltage before and after 2nd passivation layer deposition. The mean V_{th} of wafer W1 shifts by about – 0.35 V, while the shift on the wafer W2 is about -0.17 V. This confirms a higher electron density underneath the gate contacts in the case of tensile passivation. Further analyses revealed that on wafer W2 the mean value of Schottky barrier height (ϕ_b) was lowered by about 0.14 eV after passivation. K. Yao et al. [3] has proposed that Schottky contact/AlGaN interface states are responsible for strain-induced gate barrier lowering of the devices under compressive stress and vice versa. This means, the observed threshold voltage shift on the wafers was not entirely created by the direct-piezoelectric effect and ϕ_b has compensated the piezoelectric induced V_{th} shift. In Table I the changes of the analyzed DC parameters are summarized. Based on Table I we can attribute at least 0.32 V shift of V_{th} to the 1.5 GPa stress variation in the second passivation layer between wafers W1 and W2. Additionally, the intrinsic stress dissimilarity in the gate encapsulation leads to 2.8 times higher gate leakage on wafer W1 compare to W2. The lowered leakage currents on wafer W2 accompanied by the lowered ϕ_b again confirms a reduction of electron density in the case of compressive passivation layer.

As it was mentioned, the measurement results can be explained when the electron density in the vicinity of the gate

contact was enhanced/reduced. This effect is similar to the application of tensile/compressive stress on AlGaN/GaN epitaxial layers. Therefore, we propose that the mechanical force from the gate-encapsulation nitride was transferred through the gate metal stack and the first passivation layer into the area underneath the gate contact. This force depending on its polarity (compressive/tensile) either compresses or expands the semiconductor material at the interfaces, thus decreasing or increasing piezoelectric polarization respectively. This effect results in the observed difference in DC characteristics. The degree of the transferred stress depends on the device dimensions, i.e. thicknesses of the first and second passivation layers, gate length, gate-drain and gate-source distances, as well as on the mechanical properties, i.e. intrinsic stress in the deposited SiN_x and gate-metal-stack stiffness etc.

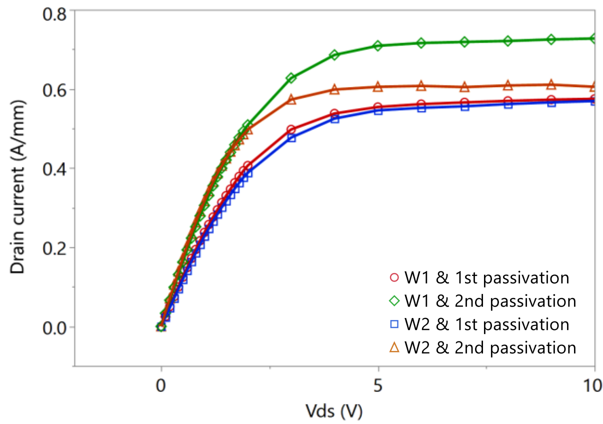

Fig. 1. Mean output characteristics for 37 transistors per wafer measured at V_{GS}= 1 V before and after deposition of the second passivation layer.

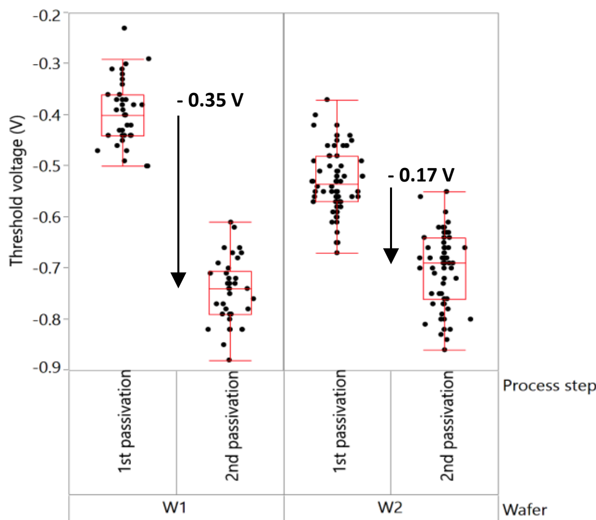

Fig. 2. Box-plot diagram is presenting the transistor threshold voltage (V_{th}) measured on wafers W1 and W2 before (1st passivation) and after (2nd passivation layer).

TABLE I
SUMMARY OF DC PARAMETERS SHIFT BETWEEN MEASUREMENTS BEFORE AND AFTER THE 2ND PASSIVATION LAYER

Parameters	Wafer W1	Wafer W2
ΔV_{th} (V)	- 0.35	- 0.17
ΔV_{th} - $\Delta\phi_b$ (V)	- 0.35	- 0.03
ΔI_{DSmax} (A/mm) (V_{DS}=10 V)	+ 0.15	+ 0.03
Gate leakage	2.35×	0.84×

SIMULATIONS

To verify our experimental results, the devices under study were simulated by Silvaco CAD tools. For this purpose, a model with dimensions representing the fabricated transistors was designed. Two cases for the second passivation in this model were considered. Device A with + 0.5 GPa tensile and device B with – 1.0 GPa compressive stressed SiN_x. The intrinsic stress in all other materials/layers was considered to be zero.

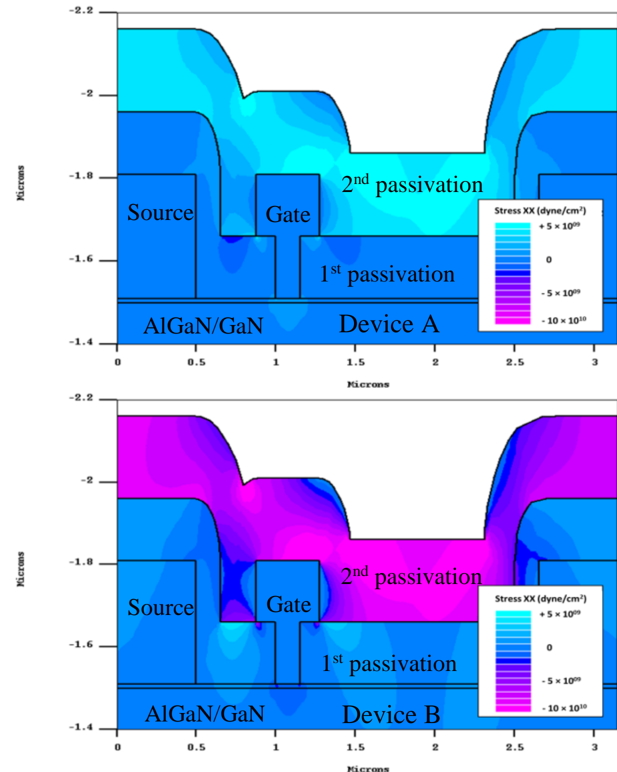

Fig. 3. Mechanical simulation (victory stress module) for devices A and B. The false colors indicate the stress.

A comparison of devices A and B in Fig. 3 shows higher stress in the device A in the area underneath the gate metallization. This is also seen in Fig. 4, which shows normal stress XX (the stress on the X plane which is caused by a force acting in the X direction) profile in AlGaN/SiN_x interface. The graph illustrates that the stress difference between devices A and B increases up to about 6 Gdyne/cm^2 (600 MPa) at the gate edges. The stress profile also shows that the transferred tension/compression is higher at the source side of the gate contact where the distance is shorter than on the drain side. Furthermore, we have noticed that besides intrinsic stress in SiN_x, the dimensions and mechanical properties of each layer vary the stress profile seen under the gate contact. For instance, it was observed that the gate head overlap over SiN_x and gate metallization stiffness vary the amplitude of stress XX. The simulation results prove the influence of the second passivation on stress profile in AlGaN/GaN epitaxial layer. This consequently has to result in a higher/lower 2DEG electron density for a tensile/compressive SiN_x respectively.

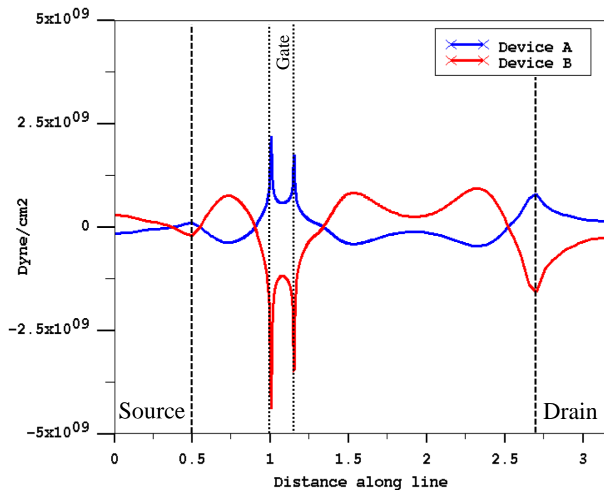

Fig. 4. Stress XX profile in the devices A and B. Cutline is selected along AlGaN/SiN_x interface.

Fig. 5 presents material displacement vectors in the device A, which has a tensile stressed layer as the second passivation. As shown in the figure a tensile nitride, i.e. an expanded material, tends to shrink. This consequently causes the forces which are directed downward (Z orientation) and applying force on the gate metallization. The displacement vectors are opposite to the gate trench opening similar to a case when the first passivation is tensile stressed. Additionally, any compression in Z direction by Poisson ratio leads to further tensile stress in X orientation. These explanations are in consistent with the observed stress XX profile in Fig. 4 for tensile/compressive passivation. The discussed forces lead to expand/contract the area underneath the gate contact which is corresponding to the devices electrical properties.

The simulation of electron density in the devices A and B is presented in Fig. 6. These images show the simulated electron density at V_{GS}= - 3 and V_{DS}= + 10 V. Comparison of the electron density underneath the gate contact indicates one order of magnitude higher density in device A, which may lead to a noticeable punch-through effect. As a consequence, higher leakage current and negative shift of pinch-off voltage for the device A are expected.

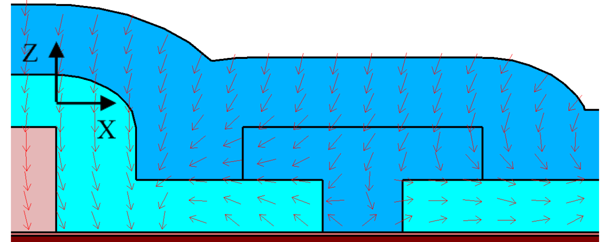

Fig. 5. Mechanical simulation of device A. The arrows are presenting the displacement in X/Z orientations in the first and second passivation layers and gate metal.

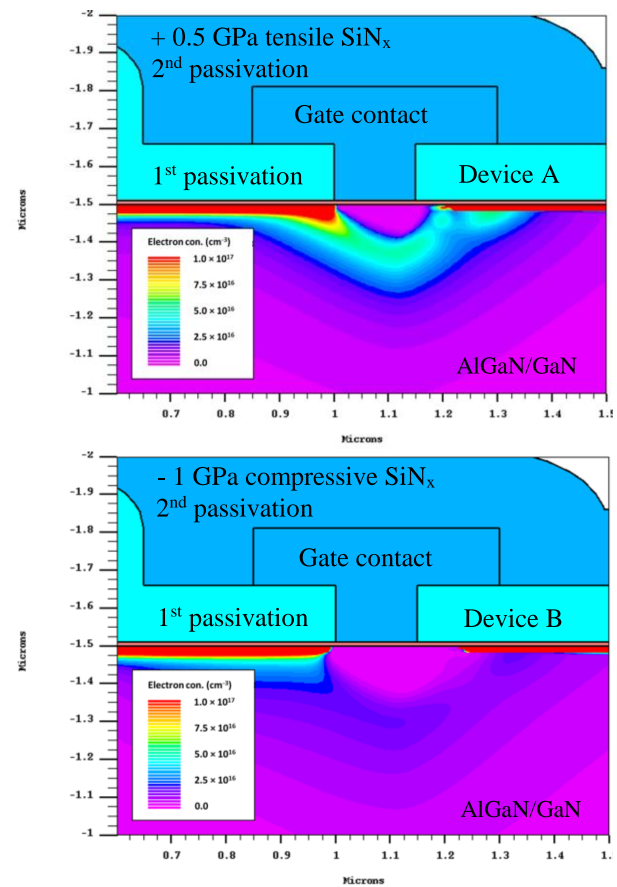

Fig. 6. Electrical simulation results for the devices A and B. Color range presents the electron density in 2DEG and GaN channel.

CONCLUSIONS

The results of our work demonstrate the importance of the intrinsic stress in SiN_x films used for the encapsulation of the gates in the fabrication of GaN HEMTs. We have shown that the mechanical strain alters the DC-characteristics of GaN HFETs after introducing intrinsically stressed nitride for the second passivation layer. This strain leads to a reduction/enhancement of the electron density in the 2DEG in the vicinity of the gate contact. As a result, gate leakage, drain current and threshold voltage were affected. This mechanism has been confirmed by simulation of the fabricated transistors showing the transferred stress to epitaxial layer and its influence on the 2DEG channel. Based on this work the intrinsic stress of the gate encapsulation layer, not necessarily SiN_x, can be effectively used for tuning the DC characteristics of GaN HFETs for particular applications. The observed changes in DC characteristics are expected to be even more pronounced for GaN-based transistors with shorter gate lengths.

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ACRONYMS

HEMT: High-Electron-Mobility Transistor
HFET: Heterostructure Field Effect Transistor
PECVD: Plasma-Enhanced Chemical Vapor Deposition
2DEG: Two Dimensions Electron Gas