GaN Through-substrate Via Process for GaN-on-GaN HEMT Power Amplifiers

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Abstract

A GaN through-substrate via (TSV) process for GaN-on-GaN HEMT power amplifiers (PAs) is described. In order to apply GaN-TSV to GaN-on-GaN HEMT PA, a thick Ni etch stop structure and a metal removal process on the dicing line were developed. Finally, GaN-TSV was applied to a GaN-on-GaN HEMT PA. The reliable connection between the etch stop and GaN-TSV was observed with a cross-sectional SEM. In CW operation, a maximum output power of 47.4 dBm (54.6 W), a maximum PAE of 63.3%, and a gain of 14.7 dB were obtained. This indicates that GaN-on-GaN HEMT PA has suitable heat dissipation properties.

INTRODUCTION

Gallium nitride (GaN) substrates are very attractive for high-frequency and high-power GaN high electron mobility transistors (GaN HEMTs) because of their potential to grow high-quality GaN epitaxial layers due to the extremely low dislocation density (10^4–10^6 cm^{-2}). We demonstrated remarkable suppression of current collapse of GaN-on-GaN HEMTs and excellent power characteristics [1]. Furthermore, a recorded power-added efficiency (PAE) of over 80% at ISM-band was obtained [2]. However, GaN substrates exhibit thermal conductivity (230 W/mK) lower than that of the widely used silicon carbide (SiC) substrates (420 W/mK) [3]. Hence, we optimized the thermal management of GaN-on-GaN using thermal simulation and found that the temperature rise was minimum at a substrate thickness of 100 μm. From these results, we developed methods for backside processing of GaN-on-GaN, such as backgrinding, CMP and dicing [4]. In addition, we developed a high-rate ICP etching for GaN through-substrate vias (TSVs) to reduce the source inductance of GaN-on-GaN HEMT power amplifiers (PAs). GaN via-holes with a depth of 91 μm were successfully fabricated with a high etch rate of 1.5 μm/min and a high etch selectivity of 35 [5]. To suppress pillar formation, increasing the wafer temperature by controlling the helium pressure for cooling was effective.

In this study, we developed a GaN-TSV process for GaN-on-GaN HEMT PAs. A 50 W-class GaN-on-GaN HEMT PA with GaN-TSVs was demonstrated. In addition, we will discuss the heat dissipation of GaN-on-GaN HEMT PAs using thermal simulation.

EXPERIMENTAL PROCEDURE

We used semi-insulating 2-in. GaN (0001) substrates with a dislocation density of less than 5×10^6 cm^{-2} (SCIOCS product), which were grown using the void-assisted separation (VAS) method with hydride vapor phase epitaxy (HVPE). GaN-HEMT epitaxial layers were grown by metalorganic vapor phase epitaxy (MOVPE) and front-side processing was performed [1, 2].

The backside process basically follows the SiC via process flow that we had developed [6, 7]. After fabricating the front-side device, thermoplastic adhesion was used to bond the wafer to a 4-in. supporting carrier. After that, the backside (N-polar side) of the GaN substrate was ground, and then CMP was performed [4]. The GaN substrate was thinned to 100 μm. An electroplated Ni metal mask with openings of 70 μm in diameter on the backside of the GaN substrate was fabricated. ICP etching was performed in a mixture of Cl_2 and BCl_3 [5]. Au electroplating was performed after seed metal sputtering. Finally, the dismounted wafer was cleaned and then diced using a stealth dicing process.

The sample was evaluated with SEM and an optical microscope. The power characteristics of the PAs were evaluated by large-signal measurement. In addition, thermal simulation was carried out to understand heat dissipation of GaN-on-GaN HEMT PAs.

GAN THROUGH-SUBSTRATE VIA PROCESS

Fig.1 shows a cross-sectional SEM image of a typical 91-μm deep GaN via-hole that was fabricated with an etch rate of 1.5 μm/min. The etching profile of the GaN via-hole has two different inclined sidewalls because of the etch back process of a Ni metal mask, which is closely related to the GaN/Ni etch selectivity [8]. The etching selectivity of GaN to Ni metal mask was 35, which was smaller than that of SiC etching (~100) [6]. Therefore, as shown in Fig. 2, it is necessary to increase the thickness of the conventional Ni etch stop. Ni with a thickness of at least 0.3 μm is required in view of the uniformity of the grinding and ICP etching of

the GaN substrate and the over-etching (10 µm). Therefore, a 0.5 µm-thick Ni etch stop structure was fabricated by electroplating. As a result, as shown in Fig. 2, the punch-through of the etch stop was not observed in the SEM observation after the GaN via etching.

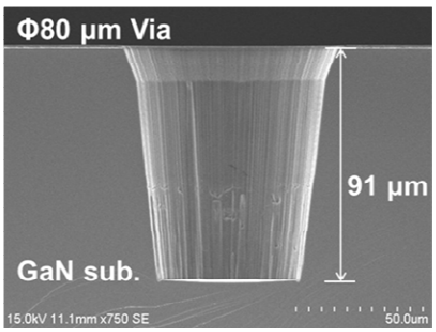

Fig. 1 Cross-sectional SEM image of a typical 91-µm deep GaN via-hole [5].

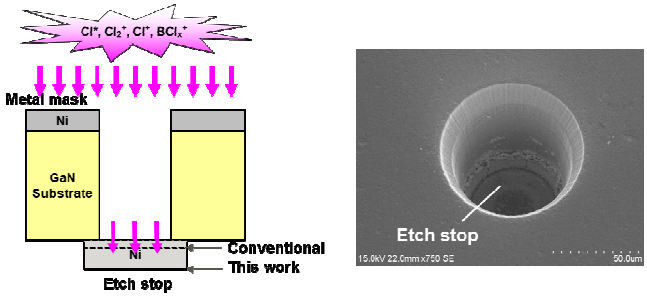

Fig. 2 Cross-sectional schematic of etch stop structure in GaN substrate via etching and SEM image of etch stop.

Stealth dicing, which involves damaging the crystal with lasers, and then expanding the crystal to separate the chips, is very effective for dicing the GaN substrate [4]. However, to separate the chips, the metal on the dicing line must be removed. Therefore, we developed a metal removal process on the dicing line that uses wet etching. Fig. 3 shows the flow of the metal removal process on the dicing line and the optical micrograph of each process. Here, a process in which Au plating is not performed on the dicing line was performed [7]. First, patterning to open the dicing line was performed to expose the surface of the seed metal (2) for Au plating on the dicing line. Next, the seed metal (2) was etched to stop etching on the Ni surface. Finally, Ni and the seed metal (1) were sequentially etched until the GaN surface was exposed, and then the resist was removed.

Fig. 4 is a photograph of a processed wafer after peeling from supporting carrier and a schematic of the dicing layout. The dicing line is indicated by light blue lines. 5-mm square chips and long chips with different widths and a length of 5 mm were involved. Fig. 5 is a chip photograph after stealth dicing. By removing the metal on the dicing line, chips of different widths facing each other were precisely divided.

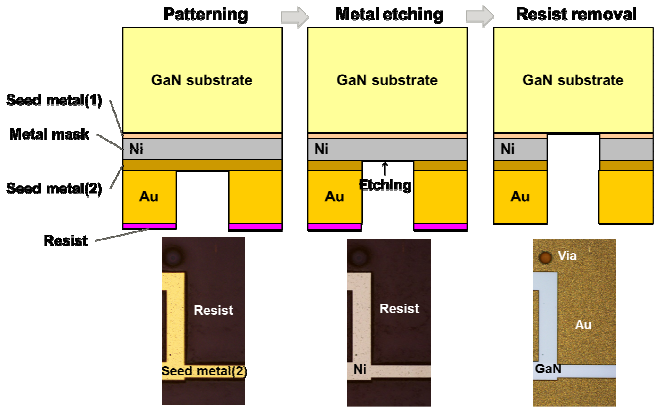

Fig. 3 Metal removal process flow on the dicing line and optical micrograph of each process.

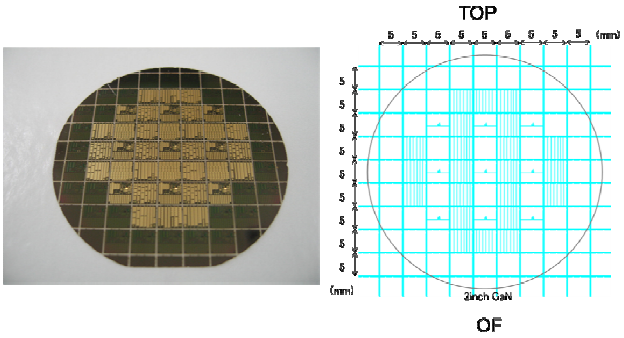

Fig. 4 Photograph of a processed wafer after peeling from supporting carrier and a schematic of the dicing layout.

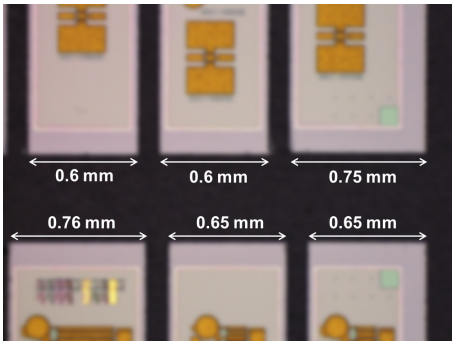

Fig. 5 Chip photograph after stealth dicing.

Fig. 6 indicates the backside photograph of GaN-on-GaN HEMT PA chip (a), and GaN-TSV SEM image (b). A plurality of GaN-TSVs, which are Au plated from the back surface of the chip to the bottom surface of the etch stop, can

be seen. Fig. 7 shows the cross-sectional SEM image of GaN-TSV of GaN-on-GaN HEMT PA. A reliable connection between the etch stop and Au plating was also observed.

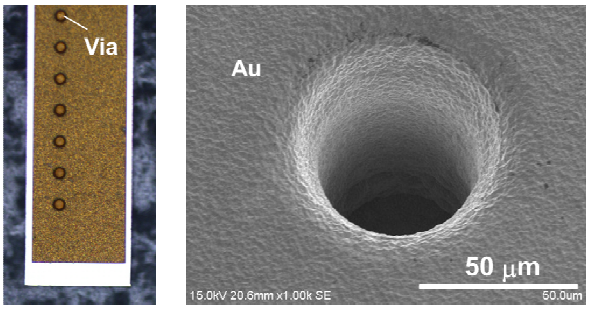

Fig. 6 Backside photograph of GaN-on-GaN HEMT PA chip (a) and GaN-TSV SEM image (b).

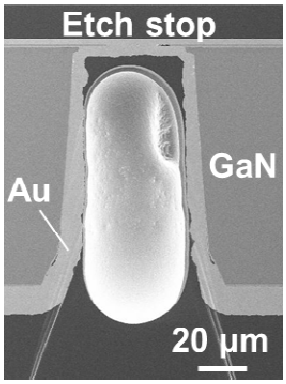

Fig. 7 Cross-sectional SEM image of GaN-TSV of GaN-on-GaN HEMT PA.

50 W-CLASS GAN-ON-GAN HEMT POWER AMPLIFIER

GaN-TSVs were applied to GaN-on-GaN HEMTs having 20-nm AlGaN barriers with an Al composition of 26% [2]. Fig. 8 shows a GaN-on-GaN HEMT PA chip mounted on an evaluation board. The evaluation board performs harmonic treatment using an input matching circuit and an output matching circuit. The GaN-on-GaN HEMT PA chip has 36 gate fingers, with a gate length of 0.5 μm and a unit gate width of 300 μm, and has a gap of 30 μm between the gates. The total gate periphery was 10.8 mm. The input matching circuit and the gate electrode pad, and the output matching circuit and the drain electrode pad are respectively connected using wire bonding. The source electrode pads were connected to the ground on the back of the chip by GaN-TSVs.

Fig. 9 shows the high-frequency power characteristics of GaN-on-GaN HEMT PA with GaN-TSVs at 2.6 GHz. GaN-TSVs connected the source and the ground without failure, enabling high-power operation without oscillation. In pulse measurement at a pulse width of 10 μsec and the duty of 1%, a maximum output power (P_{out}) of 48.1 dBm (64.3 W), a maximum PAE of 71.1%, and a gain of 15.7 dB were obtained. On the other hand, in CW operation, a P_{out} of 47.4 dBm (54.6 W), a maximum PAE of 63.3%, and a gain of 14.7 dB were obtained. The decrease in power and PAE during CW operation is due to the self-heating of the device. Fig. 10 shows a simulated comparison of the transient response characteristics of the maximum channel temperature of GaN-on-GaN HEMT PA between CW and pulse operations. As a result, the maximum channel temperature difference between CW operation and pulse operation is as large as 90 °C. However, enabling CW operation suggests that GaN-on-GaN HEMT PA has suitable heat dissipation properties.

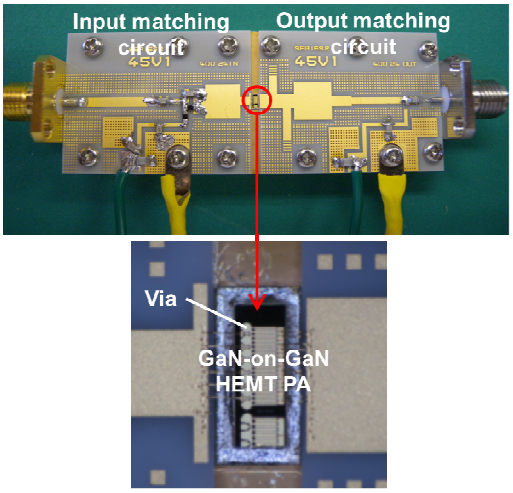

Fig. 8 Photograph of 50 W-class GaN-on-GaN HEMT PA with matching circuits.

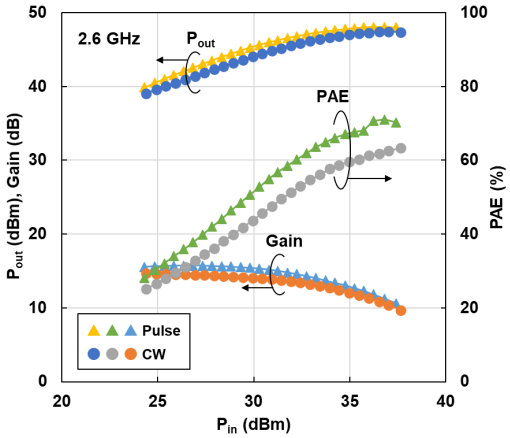

Fig. 9 Power characteristics of GaN-on-GaN HEMT PA in pulse (closed triangles) and CW (closed circles) operations.

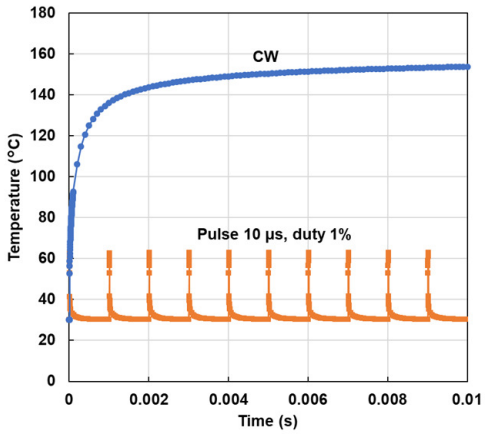

Fig. 10 Simulated comparison of transient response characteristics of maximum channel temperature between pulse and CW operations.

CONCLUSIONS

The authors studied the GaN-TSV process for GaN-on-GaN HEMT PAs, including using a thick Ni etch stop structure and a metal removal process on the dicing line. In GaN-on-GaN HEMT PAs, a reliable connection between the etch stop and GaN-TSV was observed using a cross-sectional SEM. The GaN-on-GaN HEMT PA exhibited excellent high-frequency power characteristics with a maximum P_{out} of 47.4 dBm and a maximum PAE of 63.3% in CW operation, suggesting that it has appropriate heat dissipation characteristics.

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ACRONYMS

CMP: Chemical-mechanical polishing
HVPE: Hydride vapor phase epitaxy
ICP: Inductively coupled plasma
ISM: Industrial-scientific-medical
MOVPE: Metalorganic vapor phase epitaxy
PAE: Power-added efficiency
SEM: Scanning electron microscope
TSV: Through-substrate vias
VAS: Void-assisted separation