A Systematic Approach for Determining Overlay Spec Limits in Photolithography

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Abstract

A systematic way to determine the photomask overlay spec limits by using a new overlay measurement structure is discussed in this paper. The results show that this novel artifact enabled us to automatically obtain reliable and accurate overlay measurements, monitor in-line overlay, conduct stepper alignment corrections, and establish the relationship between the misalignment and parametric test parameters. By implementing the stepper alignment corrections, the overlay control can be further improved by 30%, which ensures enough margin for high volume production.

INTRODUCTION

With increasing demands to improve the performance of HBT and pHEMT technologies and reduction in the die size for cost savings, critical dimension (CD) and overlay control in the photolithography module become more and more important. Errors in the overlay of different lithography layers can directly cause issues such as: photo rework, extra processing steps and cycle time, parametric test failures, yield loss, device performance implications, reliability concerns, and wafer scrap. However, the alignment vernier widely used has become less useful. That is because the accuracy and repeatability of reading the alignment vernier manually is quite poor. As a result, continuous improvement in overlay measurement and control is required.

In this paper, the impacts of the misalignment were analyzed. A new overlay measurement structure has been defined and implemented. An effective way to determine the overlay spec limits is discussed. The results showed the new overlay artifact provided a robust solution to improve the stepper alignment performance and made an improvement in overlay margin sustainable during high volume production.

BACKGROUND

In general, there are five major steps in photolithography. First is substrate preparation, then photoresist spin coat and soft bake, alignment and exposure of wafers on the stepper, after which comes post-exposure bake and development [(1)]. The last and critical step is post-develop-inspection, where it is determined whether the previous steps have been performed correctly and detects if the photo process yields correct critical dimensions (CDs) and good overlay. Figure 1a. shows a cross-section of a good device with perfect Via CD and overlay between layers Emitter and Via, and a bad device with oversize CD and misalignment is shown in Figure 1b. The oversize Via and misalignment resulted in the Via falling off the emitter metal, which caused die sort (DS) yield loss and reliability failures. At photo inspection step, if we can detect this kind of issue and rework the affected wafers, the yield loss can be avoided.

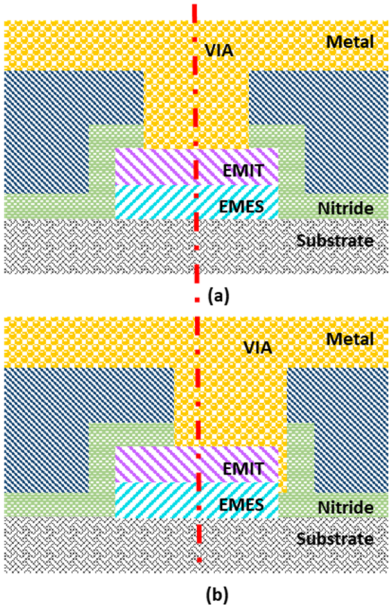

Fig. 1a. A good device with perfect CD and overlay. 1b. A bad device with oversize CD and misalignment.

Here is an example showing how the alignment affects the die sort yield (see Figure 2). The major DS yield detractor was leakage failing high. The overlay errors had dramatic impacts on the die sort test. The DS yield loss due to the misalignment on this wafer was close to 30%.

In order to better control the photo process, in addition to the critical dimensions, a successful overlay control is an essential requirement for the final performance of the devices and a critical step for maintaining a high level of yield in a wafer fab. The key point for the overlay control is to obtain accurate and precise measurement for overlay. Next, the

effective measurement of overlay errors and setting of practical limits will be discussed.

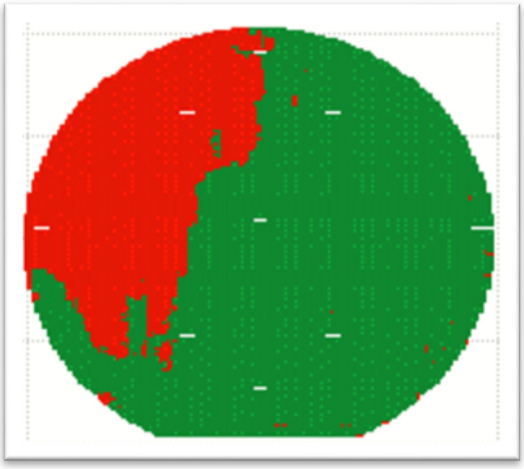

Fig. 2. Die sort yield loss (red) due to misalignment.

Description of CD and Overlay Structure

In the past, the overlay error was checked by visually reading the alignment vernier. However, numerous factors impact the manual vernier reading. Examples include microscope focus, magnification, and the person performing the measurement. It is difficult to get repeatable and accurate measurements by reading the alignment vernier. To eliminate these inconsistencies in measurement, a new metrology structure has been developed and used for automatic CD and overlay measurement by using IVS metrology system made by Inspectrology. A typical module of the new metrology row contains 1) Label, 2) CD mark, 3) Focus Mark, and 4) Overlay mark. This in-line monitoring structure for CD measurement has been implemented and proved that the measurement deviation between the standard CD artifact and the real device can be dramatically minimized [(2)]. How to obtain reliable and accurate overlay error measurements will be discussed in the subsequent sections.

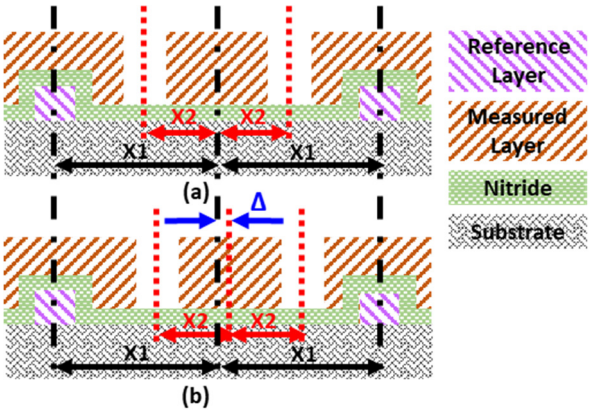

Fig. 3a. Measured and reference layers have perfect alignment. 3b. Measured and reference layers has misalignment Δ.

A standard overlay mark is shown in Figure 3. The top cross-section in Figure 3a. shows the reference layer (RL) and measured layer (ML) has perfect alignment. X1 and X2 are half the distance between the center lines of the reference features and the center lines of the measured features, respectively. The center lines of the two layers coincide. Figure 3b. shows there is a misalignment between the two layers. The center line of the measured layer has a translation error delta (Δ) in x-direction, which is called the overlay error or misalignment. The overlay error is then calculated by determining the value of the difference between the coordinates of the center line of the RL to the ML.

Results and Discussions

To pursue device performance enhancement and additional die per wafer, the feature sizes on the chip keep shrinking to decrease the capacitance, increase the gain and Fmax, and reduce the die size. At the same time, the layout design rule (LDR) between key layers is becoming more compact, such as Base-Emitter spacing, overlap between the Via and the underlying conductor, etc. This imparts huge challenges to photolithography. Next, how to implement the new overlay measurements, which enables the development of a robust process to systematically evaluate the new LDR and also determine the alignment spec limits which will improve the overlay control, will be explained.

The alignment margin experiments have been designed and performed on ASML steppers by using a mask with a new LDR and the overlay marks added. All-field overlay measurements with 5 locations (center and 4 corners) within a printfield were conducted on all wafers on the IVS metrology system. The rest of the process was unchanged. The overlay errors, PCM and Die sort data have been reviewed and analyzed.

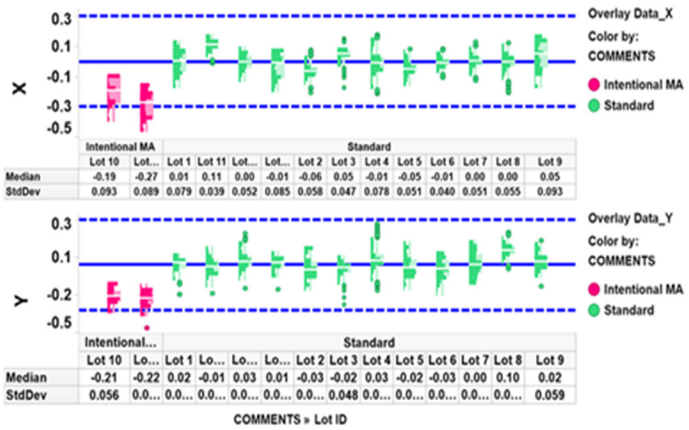

Fig. 4. An example of the overlay trend chart in X and Y directions on different lots.

An example of the overlay trend chart in X and Y directions on different lots is shown in Figure 4. Lots with the intentional

misalignment are shown in red. It was proven that the overlay errors could be found by using the new measurement approach. Therefore, the misalignment of the production lots can be well monitored.

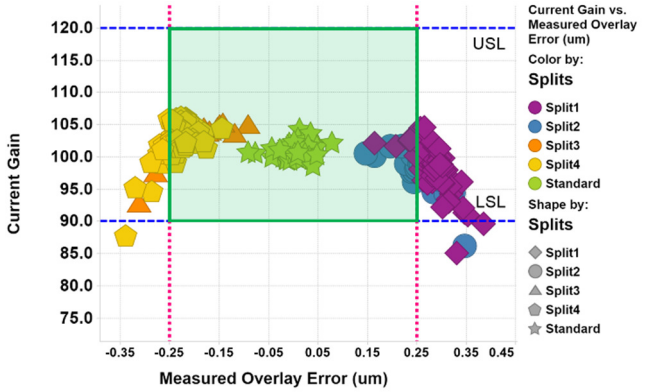

Fig. 5. The relationship between the measured overlay error and the current gain

After combining the overlay, PCM and DS data, the results show a relationship between the overlay errors and electrical test parameters. This relationship between the measured overlay error in X-axis and the current gain in Y-axis has been summarized in Figure 5. The upper spec limits (USL) and lower spec limits (LSL) for the current gain are 120 and 90 respectively. The range of alignment is from -0.35µm to +0.35µm. It can be seen clearly from Figure 5 that when the overlay error is within -0.25µm to 0.25 µm, the current gain is stable. However, it starts to roll off once the absolute value of overlay error is greater than 0.25µm. Based on the plot shown in Figure 5 and considering the current gain stability, data outside the green box should be avoided, and the misalignment must be controlled within ±0.25µm. Therefore, to meet the requirements of the new LDR, the USL and LSL for alignment should be +0.25µm and -0.25µm separately.

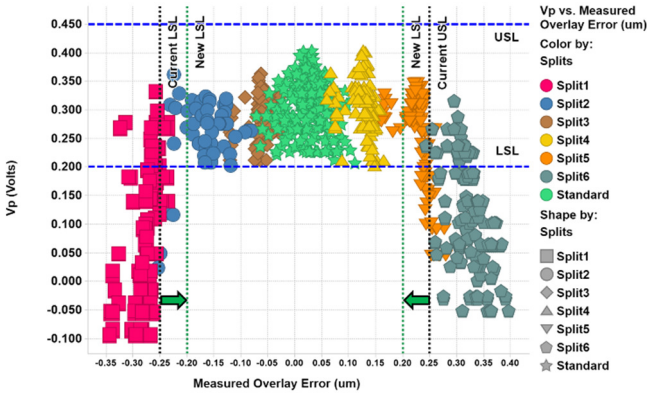

Fig. 6. The relationship between the measured overlay error and the pinch-off voltage Vp

This approach also has been used to evaluate the existing overlay spec limits. Pinch-off voltage (Vp) of pHEMT transistors is one of the key test parameters driving PCM and die sort yield. Experimental results in Figure 6 show that Egate misalignment to the wide recess (WRCS) layer (X-axis) affects Vp strongly. Vp rapidly exceeded the LSL when the overlay errors were greater than |±0.23|µm, and significant yield loss was observed. Based on the data shown in Figure 6, the current overlay spec limits of ±0.25µm would not allow acceptable process capability between Egate and WRCS alignment. Tightening the overlay spec limits from ±0.25µm to ±0.20µm is needed. The new overlay spec limits of ±0.20µm ensure that the alignment between Egate and WRCS has enough process window and yield loss can be prevented. The overlay control is critical for shipping lower PPM levels of defective die to customer. Many products depend on the overlay control to maintain good yield.

However, the capability of the tool platform only can support overlay errors from -0.30µm to 0.3µm. Running 7x24 production on steppers and controlling the misalignment ≤ |±0.25|µm seems impossible. To improve the overlay control, a team collaborated to work on the stepper alignment correction project. By analyzing the overlay data, calculating the inter-field and intra-field correction terms, and feeding back the corrections to stepper, not only the alignment requirements of ±0.25µm were met, but also allowed further tightening of the control limits for overlay error from ±0.25µm to ±0.2µm, which improved the overlay control by about 30%.

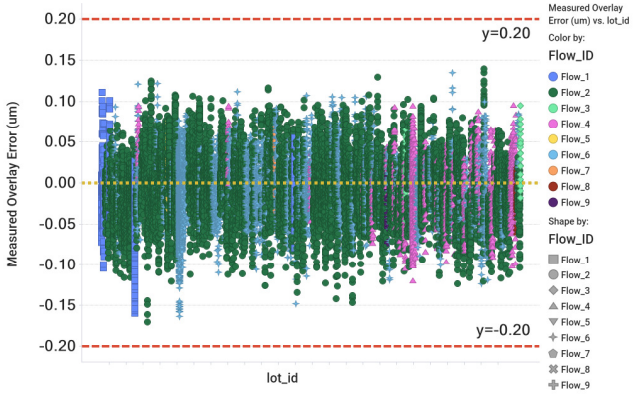

Fig. 7. The trend chart for overlay measurements

Implementing the stepper corrections, ensured that ample alignment margin in high volume manufacturing was obtained. This is demonstrated in Figure 7, which shows the overlay errors measured on 547 lots and 9 different process flows. All the individual measurement points are within the limits of |±0.20| µm. There was no rework due to misalignment. The results prove that the stepper alignment correction not only doesn't add additional production burden and increase photo rework rate, but also improves the overlay control and yield.

This paper has presented a systematic approach for determining the alignment spec limits. This allowed the limits to be set more accurately, effectively, and meaningfully. It has also been proven that the developed process ensures sufficient margin for high volume production.

CONCLUSIONS

This work has proven that the newly developed overlay measurement structure can be used for obtaining accurate and repeatable measurements, monitoring the in-line overlay, building the correlation between the overlay error and parametric test values, and establishing of the alignment spec limits effectively. In addition, significantly improved stepper alignment performance was demonstrated by the use of this novel feature. The overlay error control limits can be tightened by 30% from ±0.3µm to ±0.2µm. The results showed running 7x24 production on steppers and controlling the misalignment within ±0.20µm is feasible and practicable. This systematic and thorough alignment margin study ensures that the developed process is robust for manufacturing, yield and reliability.

ACKNOWLEDGEMENTS

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ACRONYMS

HBT: Hetero-junction Bipolar Transistor
pHEMT: Pseudomorphic High Electron Mobility Transistor
CD: Critical Dimension
PCM: Process Control Module
DS: Die Sort
LDR: Layout Design Rule
USL: Upper Spec Limit
LSL: Lower Spec Limit