Electrostatic discharge (ESD) in AlGaN/GaN HEMT due to fabrication process

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Abstract

GaN transistors have the capability of working with high voltage and high current, and GaN may be considered as ESD immune material. In this paper we shall review the root cause analysis of electrostatic discharge (ESD) defect formation and defect characterization in AlGaN/GaN HEMT wafers. An Atomic Force Microscopy (AFM) and a Focused Ion Beam Scanning Electron Microscope (FIB-SEM) cross-section revealed damage on the surface of the wafer, cracks through SiN passivation and into the AlGaN/GaN substrate. Root cause analysis investigation shows the ESD damage was formed in an automated wet chemistry fabrication process tool. An ESD formation mechanism was proposed, and its characterization and a solution to avoid it are suggested.

INTRODUCTION

Electro static discharge (ESD) is a rapid discharge event that transfers a finite amount of charge between two bodies at different potentials [1]. The amount of damage experienced in an integrated circuit (IC) is governed by the current densities and voltage gradients developed during the event. The movement of these charges occurs very rapidly, leading to high currents. When the current passes through an object, the impedance of that object establishes a voltage across it. The voltage establishes an electric field in the surrounding objects based on the geometry and dielectric material present in the structure. Both high current densities and high electric fields cause damage on semiconductor devices.

AlGaN/ GaN high electron mobility transistors (HEMT) are being use for high power application in RF frequency. Two important physical property of GaN is high critical electric field (~3.4MV/cm) and high electron concentration (~1e13 cm^{-2}). Those properties enable high breakdown voltage and high current density, which gives the possibility of generating high RF power in the transistors.

The capability of GaN IC's to work with high voltages and currents make it considered as ESD immune material. There are very few papers on ESD in GaN HEMTs and this topic been has been few interesting in the last years.

In this paper we will review the root cause analysis of ESD defect formation in AlGaN/GaN HEMT wafers due to fabrication process. An ESD formation mechanism was proposed, and the characterization of it and a solution to avoid it are suggested and implemented.

PROCESS DETAILS

AlGaN/GaN HEMTs and MMICs were fabricated on 100mm GaN-on-SiC wafers. The fabrication process started with Ti/Al/Ni/Au metal stack evaporation followed by wet chemical lift-off process. Rapid thermal annealing (RTA) at 850ºC was used to form an ohmic contact. Passivation layer of SiN is deposited by Process Enhanced Chemical Vapor Deposition tool (PECVD). Device isolation was realized by using thick photoresist and ion implantation. The photoresist was removed by aggressive plasma stripping to remove the cured resist and finished with wet chemical stripping (lift-off) processes. The isolation patterns are within 5%-10% of the wafer area depending on the MMIC design. Further process steps to realize full MMIC such as supported T-gate, field-plate, first interconnect metals, resistors, MIM capacitors, thick Au-metal with air bridge capability, back-side process with via and thick metal plating were used.

DEFECT CHARACTERIZATION

First detection of the defects was at a visual inspection station after the integrated isolation process, which is done manually by an optical microscope. Fig. 1 shows an affected metal ohmic structure. The defect was observed between two proximate ohmic contacts, and spreads all over the wafer. Another pattern found to be affected was a large metal structure, the defects concentrated at the corners of the pattern. Additional interesting observations were the defects show only at the active area of the wafer and are bounded by

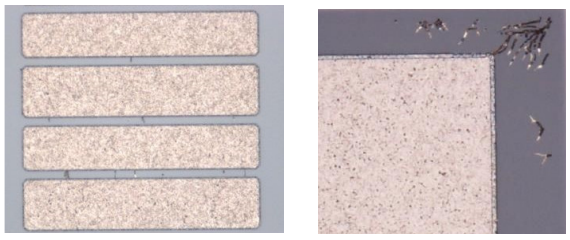

Fig. 1. Left: defect between two proximate ohmic contacts; right: defect at corner of the metal pattern, bounded by isolation layout.

the isolation layout.

Study of a transfer length method (TLM) pattern showed a direct link between the spacing length of the ohmic contacts and defect density, as shown in Fig. 2. Another observation is of similar patterns which have the same spacing, but one is not isolated between the metals (active) while the other is isolated. The active area pattern shows defects while the isolated does not, highlighting the defect characteristics described before, shown in Fig.3.

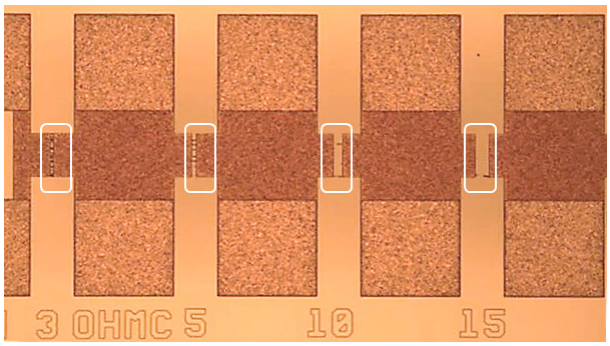

Fig. 2. TLM pattern show direct link between the spacing length of the ohmic contacts and defect density. Highest defect density is seen at 3nm spacing and the lowest density at 15nm spacing.

Fig. 3. Similar patterns have same spacing. The defect appears only at the active area.

Fig. 4 shows a FIB-SEM cross-section analysis which revealed damage on the surface of the wafer. The damage was characterized by melting channels of the SiN passivation and cracks through the AlGaN/GaN substrate. Fig. 5 shows an AFM scanning analysis, with the damage propagating into the substrate for a few hundred nanometers. The findings described in this section lead to the classification of the damage as an Electrostatic discharge defect (ESD).

INVESTIGATION OF DEFECT ORIGIN

Knowing that the first detection of the defects was at the visual inspection station bounded the search for the root cause, followed by investigation of the isolation module. This led to understanding the defect nature related to

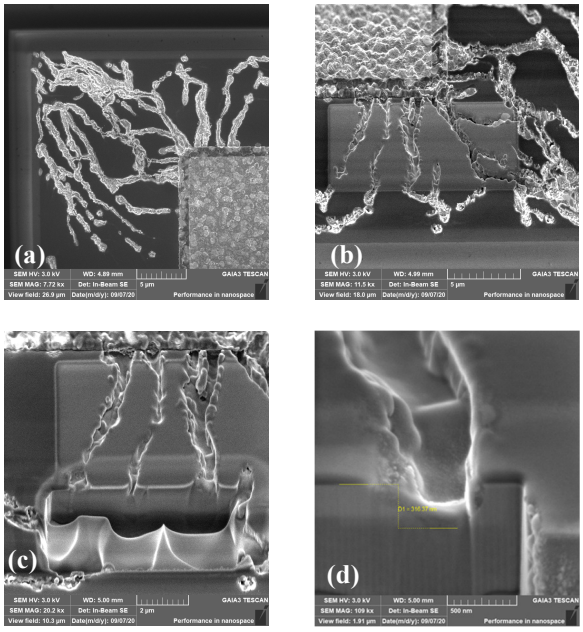

Fig. 4. FIB-SEM images of defect, (a) Top view, (b) Tilt view, (c) cross-section, (d) cross section and crack's depth measurement

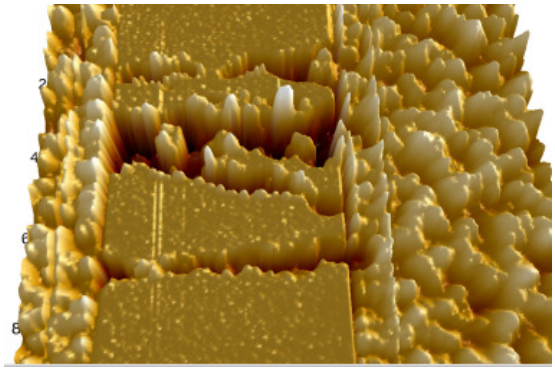

Fig. 5. AFM scanning of the surface of the wafers between two proximate ohmic contacts shows cracks.

electrostatic discharge, which limited the suspects to tools prone to causing this kind of defects. Tools in the process flow that have the highest probability for ESD related defects such as the implantation tool and those involving plasma were immediately marked as the main suspects. Commonality analysis disproved the RIE tool and pointed to one of the wet chemical lift off tools as a possible source. The investigation started with the implant tool. The implant process has been done at a vendor site. All the affected wafers fabricated in a sequence at the same day and no other wafers ran since the damaged batch to acquit the implant tool. Looking into data logs of the implant tool and comparing main process parameters of the affected wafers to base line wafers, highlighted the beam current parameter

was on the lower zone of its trend chart over the relevant period of time. An experiment was initiated to identify the origin of the defect focusing on implementation process. Five wafers were processed at the implant tool at three different beam currents set points to test the process window; low, base line and high set point values. The first assumption was that the wafers that were processed at the lowest beam current set point will show the highest magnitude of damage. However, visual inspection after the implant process wafers experiment did not show any signs of ESD damage. This finding weakened the assumption the implant process is the source for the defects, and moved the attention to the lift off machine. The next step in the flow is photo resist striping by the lift off machine. Wafers were processed in sequence, one by one and split between two wet stations. Station A is a batch immersion lift off tool, station B is a single wafer high pressure solvent spray tool. Summary of ion beam currents implantation process conditions, lift off tool types and the observations of a visual inspection are listed in Table 1. Both wafers which processed in tool B showed clearly ESD defect which points to it as causing the defect. Following this distinction, it was clearly required to delineate the scope of the damage and review wafers passing through this tool, seeking for ESD typical characteristic defects and to determine the starting time point of the problem. Several defected wafers were found in line at advance modules showing this defect in a low magnitude. Wafers pass through this tool at several steps in process flow, although only wafers which processed at Isolation module showed this defect. Examination of the process parameters of the different module's recipes showed the primary difference between them is the spray high pressure set point. At the Isolation module, pressure set point was the highest comparing to other recipes. Moreover, referring to tool A, which uses different resist stripping techniques, also reinforced suspicion to pressure related root cause for defect formation. To confirm this suspicion wafers were processed in tool B with lower pressure set points and did not show any evidence for ESD defects. Following this, wafers were processed in the tool at high pressure and gave clear signature the damage is caused only at high spray pressure condition.

TABLE I.
A SUMMARY OF BEAM CURRENTS CONDITIONS, LIFT OFF TOOLS AND OBSERVATION OF DEFECTS.

Wafer	**Beam Current**	**Lift Off Tool**	**Defect Observation**
1	High	A	No
2	High	B	Yes
3	Low	A	No
4	Low	B	Yes
5	Base Line	A	No

DISCUSSION OF DEFECT MECHANISM

Studying the tool's configuration and process details were necessary to establish a possible model for defect formation root cause. The tool combined two process techniques; first module is a heated emersion processing and second module is a single wafer high pressure spray process. Following the soak the solvent wet wafer is transported to a single wafer spin process station for lift off processing. Most of the resist dissolved during the soak, and the cured resist residues are rapidly removed with high pressure process that includes fan spray of NMP. First to be inspected was the grounding of all relevant parts in the tool. Several parts were found ungrounded. After repairing the faults, wafer was processed and still showed ESD defect. This result lead to a model related to ESD generation due to friction between high speed liquid and nozzle surfaces. Static electricity can be generated between the liquid and the pipe wall when the liquid flows inside the pipe or can be generated by being ejected from the nozzle. In high pressure there is a critical spray droplet speed which can result in static electricity, when the charged fluid impacts the wafer surface it is discharging and it causes ESD defect on the surface of the wafer [2]. This model can describe the defect formation mechanism in this case. As described, the tool uses high pressure lift off technique. High speed flow of NMP is ejected from narrow nozzle and generates static electricity, shown in Fig. 6. The charged droplet strikes the surface of the wafer, the metal patterns on the active area on the wafers are charged and being discharged in conductive areas which are patterned by the isolation process. To avoid this defect, spray pressure was decreased to an optimum value and defect was eliminated.

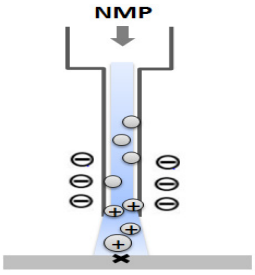

Fig. 6. A diagram of static electricity generated between the liquid and the pipe wall.

CONCLUSIONS

This paper demonstrated an ESD damage formation in AlGaN/GaN HEMT wafers due to the fabrication process. By using root cause analysis the source of the ESD damage was identified and a model was proposed. A lift-off tool with high pressure capability caused fluidic discharge when impacts the wafer surface. To avoid this defect spray pressure was decreased to an optimum value and defect was eliminated.

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ACRONYMS/NOMENCLATURE

ESD: Electro Static Discharge
GaN: Gallium Nitride
HEMT: High Electron Mobility Transistor
TLM: Transfer Length Method
FIB-SEM: Focussed Ion Beam milling combined with Scanning Electron Microscopy
AFM: Atomic Force Microscope