Low-temperature direct wafer bonding innovating CS device technologies

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Abstract

Direct bonding of wafers is attractive in integrating dissimilar materials into advanced devices and modules, because different materials can be directly bonded at room temperature. Surface activated bonding (SAB) is especially promising, because wafers are bonded at room temperature, and no wet processing is required. The bonding quality is sensitive to the wafer morphology and flatness, because bonded interfaces are formed without intermediate layers. In the first step of the SAB process, the wafer surfaces are activated by irradiation with a fast atom beam (FAB). We discuss the effects of wafer morphology on bonding quality. We will describe the effects of FAB irradiation on the nanostructural and electrical properties of the bonded interfaces. We will also show recent results of direct bonding of diamond. This exciting result offers a new path for innovation in compound semiconductor technologies.

INTRODUCTION

Heterogeneous integration of dissimilar materials has achieved a great progress in the compound semiconductor industry, and it has enabled fabrication of several types of heterostructure devices. Direct bonding technologies performed at room temperature enable the integration of dissimilar materials with different lattice constants, crystal structures, and coefficients of thermal expansion [1] into exciting new device types which would otherwise be impossible to create. Among the several types of direct bonding technologies, surface activated bonding (SAB) is especially promising, because bonding can be achieved without any wet processing, and successful bonds can be formed at room temperature, without heating the wafers [2]. Various combinations of dissimilar materials have been successfully bonded, and the structural and electrical properties of the bonded interface have been characterized.

Here, we will focus on SAB as a method for fabricating novel semiconductor devices. After outlining the SAB process, we will discuss the requirements for successful wafer bonding, and describe the effects of different surface activation conditions on the properties of the bonded interface. The fabrication and characterization of junctions fabricated by direct bonding of diamond will also be described.

METHODS AND EFFECTS OF SURFACE ACTIVATION

Figure 1 shows the process flow of surface activated bonding (SAB). First, wafers are loaded into a vacuum chamber, and a fast atom beam (FAB) of neutralized atoms (typically Ar) is used to remove the native oxide on the wafer surfaces. The pressure and acceleration voltage during FAB are ~10^{-6} Pa and 1-2 kV, respectively. The activated surfaces of the two wafers are then bonded, by pressing them together with a bond pressure of ~10 MPa.

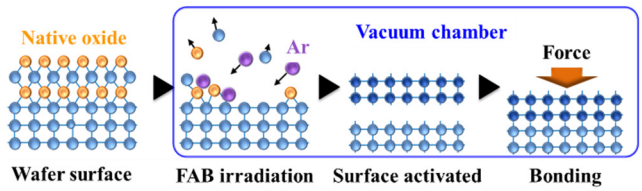

Fig. 1. Schematic process flow of surface activated bonding.

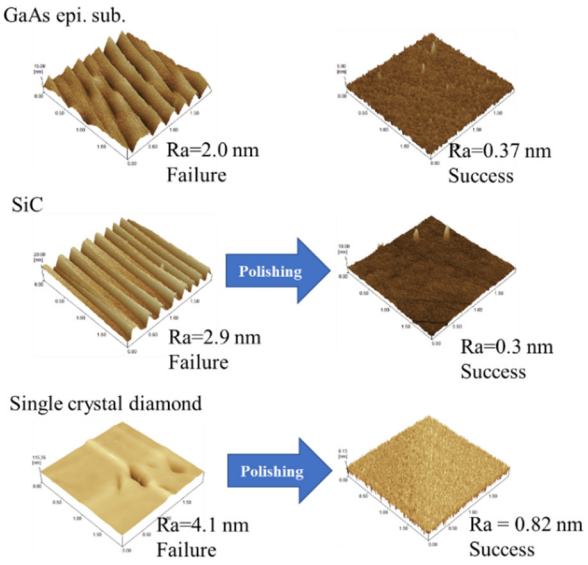

Fig. 2. AFM images and results of bonding test of wafers.

The bonding yield is sensitive to the wafer morphologies, including large scale flatness, bowing, and localized roughness. One empirical criterion is that the roughness average (Ra) of bonded surfaces should be <1 nm for successfully bonding semiconductor wafers. Assessing this

criterion can be done using an atomic force microscope. (AFM) images of several wafers used in the bonding test are shown in Fig. 2. The undulation of wafer surfaces observed in off-angle wafers degrades bonding yield, so it should be avoided. Other wafer surface morphology characteristics such as warp and thickness variation will often limit the bonding yield.

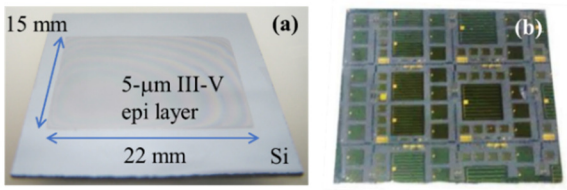

Fig. 3. (a) 5-μm III-V epi layer bonded to Si. (b) InGaP/GaAs/Si hybrid triple-junction solar cells [3].

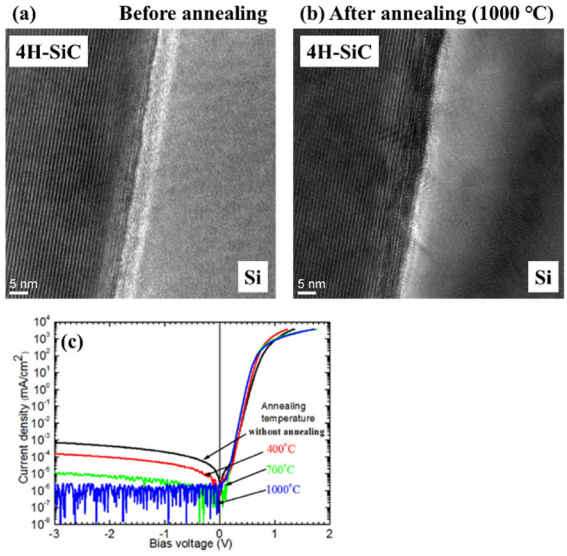

Fig. 4. TEM images of (a) as-bonded and (b) 1000-°C annealed p^+-Si/n-4H-SiC interfaces. (c) Current-voltage characteristics of p^+-Si/n-4H-SiC junctions annealed at different temperatures [4].

The surfaces of the wafers are etched slowly by sputtering during the FAB irradiation with Ar. The etch rate of Si is typically 2-3 nm/min. The surface roughness Ra increases for longer durations of FAB irradiation. The FAB duration and flux must be optimized; enough FAB to remove surface oxides and provide surface activation, but not so much as to excessively erode the surface. Using the optimized bonding conditions, we successfully prepared 5-μm thick III-V epi layer/Si junctions by bonding epi layers grown on GaAs (100) wafers to Si and selectively etching the GaAs wafers (Fig. 3(a)). InGaP/GaAs/Si hybrid triple-junction solar cells were fabricated using the III-V/Si junctions as is shown in Fig. 3(b) [3].

We observed amorphous-like layers and/or defect layers in the vicinity of as-bonded interfaces using transmission electron microscope (TEM) [4,5]. Deviation from stoichiometry was apparent in GaAs layers near as-bonded GaAs/Si interfaces [5]. In most cases such damaged layers caused by the FAB irradiation, become faint after annealing the junctions, as is typically seen in TEM images of Si/4H-SiC (Figs. 4(a) and (b)) [4] and GaAs/Si interfaces [5].

Damage due to FAB irradiation will introduce midgap defect states at the bonded interface, and will cause degradation in their electrical properties. The reverse leakage current observed p^+-Si/n-4H-SiC junctions was reduced by annealing them at 1000 °C (Fig. 4(c)) [4]. We also found that resistance across n^+-GaAs/n^+-Si junctions decreased from ~30 to 1.6-2.1 mΩcm^2 after annealing [6]. These results show that post-bonding annealing can improve the quality of junctions formed by SAB bonding. (This effect is analogous to the annealing induced reduction in damage and junction leakage currents seen after plasma damage in junctions from conventional dry etching.

RECENT ACHIEVEMENTS—DIRECT BONDING OF DIAMOND

Semiconductor devices and modules with extremely low thermal resistance can be realized by directly bonding either semiconductors or metals (heat sink) to diamond, i.e., by employing the "X-on-diamond-on metal" configurations (Fig. 5). First, we directly bonded a Ib-type single crystal diamond to a Si (100) wafer. The diamond was firmly bonded to the Si wafer, even after annealing at 1000 °C, despite the large mismatch in the coefficients of thermal expansion [7].

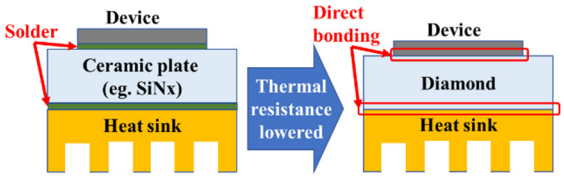

Fig. 5. Modules with direct-bonding based "X-on-diamond-on metal" configuration targeting the lowest thermal resistance.

We successfully fabricated FETs by the epitaxial growth on bonded diamond wafers and device fabrication process shown in Fig. 6. The substrate temperature during the epitaxial growth was as high as ~930 °C. The bonded Si/diamond junctions were stable against such a high temperature process. The TEM images (Fig.7) show that SiC intermediate layers formed at the bonded interfaces after annealing, which might explain the unexpectedly excellent tolerance of these junctions against thermal process.

We also bonded a 200-nm p-GaAs epi layer to diamond, and characterized the nanostructures of the bonded interface, before and after annealing at 400 °C. TEM images of interfaces before and after annealing are shown in Figs. 8(a) and 8(b), respectively. In contrast to other interfaces, defect layers observed in the as-bonded interface remained even after annealing, which suggests that the condition for surface

activation should be optimized for improving interface characteristics by post-bonding annealing.

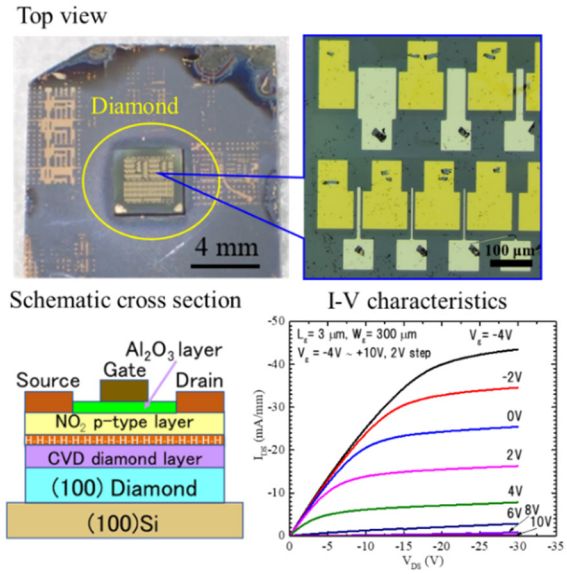

Fig. 6. Top view, schematic cross section, and current-voltage characteristics of diamond FETs fabricated on diamond bonded to Si (100) wafer [7].

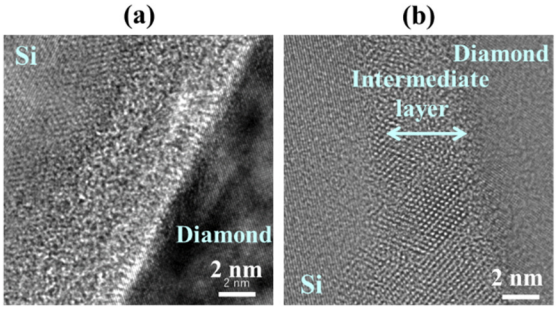

Fig. 7. TEM images of (a) as-bonded and (b) 1000-℃ annealed Si/diamond interfaces.

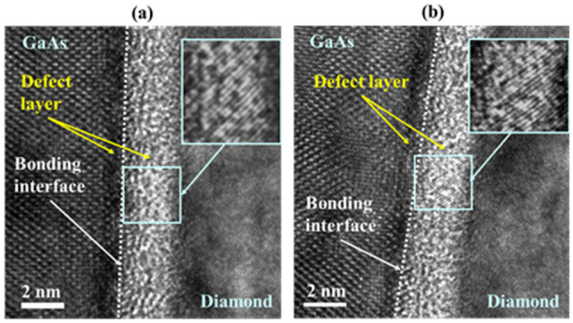

Fig. 8. TEM images of (a) as-bonded and (b) 400-℃ annealed GaAs/diamond interfaces [8].

The thermal properties of the GaAs layers were characterized by observing infrared (IR) emission from surfaces, while varying bias voltages parallel to GaAs/500-μm diamond interfaces. Results are summarized in Figs. 9(a) to 9(e). The observed thermal resistance of the GaAs/diamond junction (6 K/W, which corresponds to ~1.4×10^{-7} m^2·K/W by normalizing using the GaAs mesa area for heat dissipation, 60 μm by 400 μm) was smaller than that of GaAs/370-μm sapphire junction (34.9 K/W (~8.4×10^{-7} m^2·K/W)), because of the much higher thermal conductivity of diamond (~2000 W/mK) compared with sapphire (41 W/mK) [8]. The measured thermal resistance was comparable to approximate estimates of thermal resistance (1.4 and 54 K/W for GaAs layers on diamond and on sapphire, respectively). Our research has now been extended to direct bonding of GaN and diamond for fabricating GaN-on-diamond structures without intermediate layers. The nanostructural properties of GaN/diamond interfaces, and their thermal resistances are now under investigation.

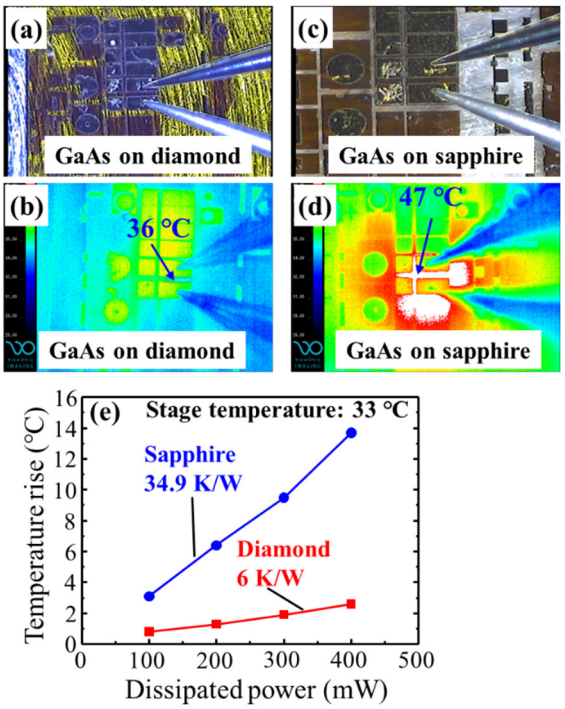

Fig. 9. (a)-(d) IR images of GaAs layer on diamond and GaAs layer on sapphire. (e) Relationship between temperature and dissipated power for GaAs layers [8].

Promising results have been obtained by bonding metals to diamond. Cu/diamond junctions were fabricated and their thermal properties were characterized. As is seen from TEM images (Figs. 10(a) to 10(c)), defect layers were apparent at as-bonded Cu/diamond interfaces. The thickness of these defect layers decreased by annealing junctions at 700 ℃. Using time-domain thermal reflectance, the thermal boundary resistance (TBR) of the bonding interfaces was estimated to be (1.7±0.2)×10^{-8} m^2·K/W [9], which was close to that of evaporated Cu/diamond interfaces and ~1/10 of TBR of solder layers (Fig. 10(d)).

These results show that direct bonding technologies, such as SAB, are very promising for realizing advanced high power CS devices and modules with very low thermal resistance.

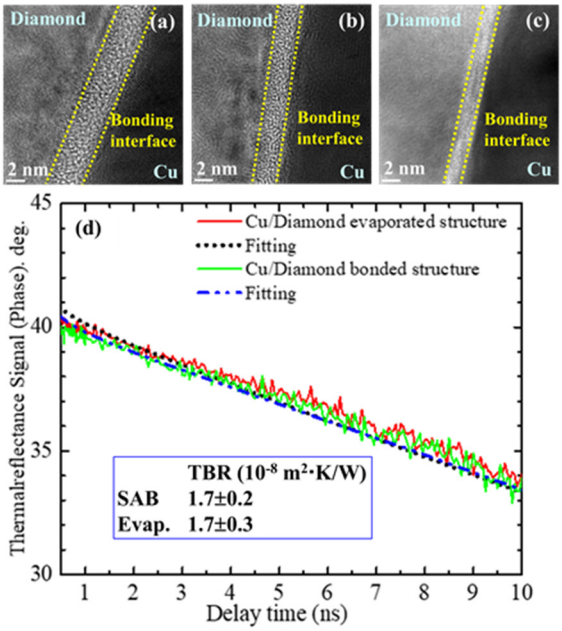

Fig. 10. TEM images of (a) as-bonded, (b) 500-°C annealed, and (c) 700-°C annealed Cu/diamond interfaces. (d) Thermal reflectance signals of Cu/diamond bonding interface and evaporated Cu/diamond interface [9].

SUMMARY

Results from several applications of surface activated bonding (SAB) were described, with emphasis on characteristics of fabricated semiconductor junctions. The influence of wafer flatness and morphology on bonding yield were described. The effects of Ar FAB beam irradiation on the nanostructural and electrical properties of the bonded interfaces were discussed. We showed that post-bonding annealing plays an important role in improving structural and electrical quality of the bonded interface. Recent exciting initial results of bonding of diamond to other semiconductors and metals were presented. This work is ongoing and more will be reported in future publications.

ACKNOWLEDGEMENTS

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ACRONYMS

AFM: Atomic Force Microscope
FAB: Fast Atom Beam
Ra: Roughness average
SAB: Surface Activated Bonding
TBR: Thermal Boundary Resistance
TEM: Transmission Electron Microscope