Application of MOS Technology to Silicon Carbide Devices

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Outline

• Introduction
• MOS Fundamentals
  • Kinetics
  • Process Technology
  • Characterization
• Historical Progress
• Future Prospects
• Summary and Discussion
What is MOS?

Metal \quad \text{Oxide} \quad \text{Semiconductor}

\text{SiO}_2 \quad \text{p-Si}

\begin{align*}
\Delta C &= 3.15 \text{ eV} \\
\Delta V &= 4.7 \text{ eV}
\end{align*}
Why is MOS Important?

Field Effect Switching; Charge Storage

Metal  Oxide  Semiconductor

$+V_G$

$E_C$

$E_F$

$E_i$

$E_V$

$V_G$

$E_F$
Si Devices Enabled

- **Switching Devices**
  - NMOSFET
  - PMOSFET
  - CMOS
  - LDMOS
  - Power MOSFET
  - IGBT

- **Charge Storage/Transfer**
  - DRAM
  - CCD

MOS Structures can be made on SiC thereby enabling all of these devices on SiC as well.
Kinetics of Oxide Growth

\[ \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \text{ (Dry)} \]
\[ \text{Si} + \text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2 \text{ (Wet)} \]

\[ T = 1000^\circ\text{C}, \text{ Dry O}_2 \]
\[ T_{\text{OX}} = 500\text{Å} \text{ (t=1 hr)} \]

\[ \text{E}_A = 28.5 \text{ kcal/mol} \]
\[ \text{E}_A = 46.6 \text{ kcal/mol} \text{ (Si-Si)} \]

\[ \text{SiC} + 3\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 3\text{H}_2 + \text{CO} \]

\[ T = 1200^\circ\text{C}, \text{ Dry O}_2 \]
\[ T_{\text{OX}} = 500\text{Å} \text{ (t=2.5 hr)} \]

\[ \text{E}_A = 34 \text{ kcal/mol} \]
\[ \text{E}_A = 58 \text{ kcal/mol} \text{ (Si-C)} \]
Transition to SiO$_2$

SiO$_2$

Amorphous SiO$_2$

$\text{SiC}_y\text{O}_x$, $t_{\text{int}} \sim 50 \text{ Å}$

4H-SiC

SiC
MOS Process Flow

Fabrication of Si MOS Capacitor

- Incoming clean
  - Solvent Clean
  - Piranha Clean
- Pre-Oxidation clean
  - Organic Clean (DI:NH₄OH:H₂O₂)
  - Metal Clean (DI:HCl:H₂O₂)
  - Oxide Etch (DI:HF)
- Immediately load into furnace
  - Low temperature push
  - Oxidation/Anneal at high temp
  - Low temperature slow pull
- Immediately metallize
  - Blanket Al evaporation
  - Photolithography
  - Etch
- Clean backside
  - Frontside PR protect
  - Oxide Etch (DI:HF)
  - PR Strip
- Forming Gas anneal
  - 450°C 30 min
  - H₂ containing ambient
MOS Process Flow

Major Differences for SiC

- Ozone clean prior to pre-oxidation clean
- Furnace push occurs with Dry O$_2$ flowing
- Low temperature Wet O$_2$ prior to ramp up
- Oxide growth at $T > 1100^\circ$C
- Low temperature Wet O$_2$ after oxide growth
- High temperature nitridation needed as final step
- Forming Gas anneal not as effective
Characterization of MOS Structures

Non-Idealities: $\Delta_{MS}$

- $\Delta_{MS} = \Delta_{M} - \Delta_{S} = -0.86\,\text{eV}$

- Vacuum Level: $\Delta_{M} = 4.1\,\text{eV}$
- SiO$_2$: $\Delta_{Si} = 4.05\,\text{eV}$
- p-Si (1E16 cm$^{-3}$): $\Delta_{S} = \Delta_{Si} + \frac{E_G}{2} + \Delta_{F} = 4.96\,\text{eV}$
Characterization of MOS Structures

Non-Idealities: $\Phi_{MS}$

Net Effect:
Constant Shift in Voltage

$\Phi_{MS} = \Phi_M - \Phi_S = -0.86\text{eV}$
Characterization of MOS Structures

Non-Idealities: $Q_{OX}$

Net Effect:
- Constant Shift in Voltage
- Mobility Reduction

+ $Q_{OX}$ is balanced by ionized acceptors

Metal | Oxide SiO$_2$ | Semiconductor p-Si
Characterization of MOS Structures

Non-Idealities: $D_{IT}$

- Net Positive Charge
  - charge if filled, neutral if empty
  - + charge if empty, neutral if filled

Metal | Oxide $\text{SiO}_2$ | Semiconductor $\text{p-Si}$

$E_F$, $E_C$, $E_i$, $E_F$, $E_V$
Characterization of MOS Structures

Non-Idealities: $D_{IT}$

Net Effect:
Variable Shift in Voltage
Mobility Reduction

Net Negative Charge
- charge if filled, neutral if empty
+ charge if empty, neutral if filled

Metal  Oxide  Semiconductor
|       | SiO₂   | p-Si   |

$E_F$, $E_C$, $E_i$, $E_F$, $E_V$
RT Photo C-V

P-SiC MOS-C, HP4284 100kHz

Capacitance (pF)

Voltage (V)

accumulation
flatband
interface state ledge
inversion
light on/off
deep depletion

$T_{OX} = \frac{\Box_{OX} A}{C_{ACC}}$

$Q_{OX} = \frac{C_{OX} (\Box_{MS} \Box V_{FB})}{qA}$

$N_A = \frac{2}{q \Box_{SiC} A^2 \frac{d(1/C^2)}{dV}}$

$D_{IT} = \frac{C_{OX} \Box V}{qAE_G}$
Simultaneous NMOS-PMOS CVs

$C_{FB}$

Ideal

$Q_{MS}$

$Q_{OX}$

$Q_{IT}$
NMOS-PMOS CV Yields Interface Quality

\[ V = E_{\text{FN}} + E_{\text{FP}} + V_{\text{IT}} \]

\[ V_{\text{FB}} = V_{\text{OX}} + V_{\text{IT}} \]

Capacitance (F) vs. Gate Voltage (V)
High-Low C-V

N-SiC MOS-C, Keithley 590, 595, 5951

Capacitance (pF)

Gate Voltage (V)

\[ D_{IT} = \frac{C_{OX} C_{LF}}{C_{OX} + C_D} \frac{C_{OX} C_{IT}}{C_{OX} + C_{HF}} \frac{1}{qA} \]

\[ C_{HF} = \frac{C_{OX} C_D}{C_{OX} + C_D} \]

\[ D_{IT} = \frac{C_{OX} C_{LF}}{C_{OX} + C_D} \frac{C_{OX} C_{HF}}{C_{OX} + C_{HF}} \frac{1}{qA} \]
High-Low C-V

Energy Calculation

\[
E \square E_V = \frac{E_G}{2} \square \square F + \square S
\]

\[
\square F = kT \ln \left( \frac{N_A}{n_i} \right)
\]

\[
W_D = \frac{\square_{SiC} A}{C_D}
\]

- \( D_{IT} (x 10^{11} \text{cm}^{-2}\text{eV}^{-1}) \)
- \( E - E_V (\text{eV}) \)
- \( E_C, E_i, E_F, E_V \)
- \( \square F, \square S, W_D \)
- \( n_i, N_A \)
- \( kT, q \)
- \( C_D, \square_{SiC} \)
- \( E_G \)
Conductance Technique

P-SiC MOS-C, HP4284

1. Bias MOS-Capacitor into strong accumulation
   a. Measure $C$ and $R$ in series mode ($C_{OX}$ and $R_S$)
   b. Sweep frequency (100 Hz to 1 MHz)

2. Bias MOS-Capacitor into flatband
   a. Measure $C$ and $R$ in parallel mode ($C_M$ and $G_M$)
   b. Sweep frequency (100 Hz to 1 MHz)

3. Bias MOS-Capacitor toward depletion
   a. Measure $C$ and $R$ in parallel mode ($C_M$ and $G_M$)
   b. Sweep frequency (100 Hz to 1 MHz)
Conductance Technique

P-SiC MOS-C, HP4284

\[
\begin{align*}
G_p = & \frac{qD_{IT}}{\sqrt{2 \ln[1 + \left( \frac{e}{2} \frac{C_{US}}{C_{US}} \right)]}} \frac{U_S^2}{e^{2U_S}} dU_S \\
C_C = & \frac{G_c C_M}{a} \\
G_C = & \frac{a(G_M^2 + \square^2 C_M^2)}{a^2 + \square^2 C_M^2} \\
a = & G_M \square R_S (G_M^2 + \square^2 C_M^2) \\
G_P = & \frac{\square C_{OX}^2 G_C}{G_C^2 + \square(C_{OX} \square C_C)^2}
\end{align*}
\]

Conductance Technique

Energy Calculation

\[ C_{IT} = \frac{qD_{IT}}{\sqrt{2\frac{U_s^2}{US}}} \arctan \left( \frac{U_s}{\frac{U_s^2}{2US}} \right) e^{\frac{U_s^2}{2US}} dU_s \]

\[ C_D = C_p \square C_{IT} \]

\[ C_p = \frac{\Box^2 C_{ox} C_C (C_{ox} \square C_C) \square G_C^2 C_{ox}}{G_C^2 + \Box (C_{ox} \square C_C)^2} \]
Comparison of Results

High-Low and Conductance

- \( D_{IT} \) measurements can only be made in the majority carrier half of the bandgap
- High-Low is easier for analysis and allows deeper probe of bandgap
- Conductance is easier to implement, has greater sensitivity, and yields data on trap dynamics
Simple Lateral NMOSFET Fabrication

400 µm x 400 µm Channel

- B-doped Poly-Si
- 500 Å SiO₂
- Inverted Channel
- P⁺ 4H-SiC Substrate
- Backside Contact
Simple Lateral NMOSFET Characterization

$C_G - V_G$ with Source, Drain, Body Grounded

Gate Capacitance ($C/C_{OX}$)

- Accumulation
- Flat Band
- Depletion
- Inversion
- Filling Traps
- Fully On
- Turn On

Gate Voltage (V)
Simple Lateral NMOSFET Characterization

Field Effect Mobility Measurement

\[ I_D = \frac{W}{L} \frac{\sqrt{nC_{OX}}}{A} (V_G - V_{TH}) V_D \frac{V_D^2}{2} \]

\[ \frac{\partial I_D}{\partial V_G} = \frac{L}{W} \frac{A}{C_{OX} V_D} \frac{\partial I_D}{\partial V_G} \]
Reliability Concerns in the DMOSFET

Relevant Oxide Fields

ON State ~NMOS

OFF State ~PMOS

Gate Oxide

Gate Metal

Ni

N-Type Source

P-Well

N-Type Drift Layer

N-Type Substrate

V_D ↑

V_G ↑
Reliability Method

Time Dependent Dielectric Breakdown

- Simultaneously stress capacitors (each 200 μm in diameter) into strong accumulation at a desired operating temperature
  - N-type: Positive stress; P-type: Negative stress
- Record failure times for all capacitors
- Determine time at which half the distribution has failed (MTTF) for a given oxide field
- Plot MTTF vs. Field and extrapolate back to lower fields to determine reliability
Reliability Method

Constant Voltage Stress

- Large enough accumulation bias to collect data in reasonable amounts of time
- Constantly monitor current until failure criterion is attained.
- Computer collects failure statistics
Reliability Method

Dielectric Strength Measurement

- **Fowler-Nordheim Tunneling**
- **SiO$_2$**
- **SiC**
- **$E_C$**

![Diagram showing dielectric strength measurement with log gate leakage vs. gate oxide field.](image)
Reliability Method

Weibull Plot of Intrinsic Failures

Field (MV/cm) → 8.1  7.6  7.1

Cumulative Failure (%)

Failure Time (sec)

50

2.5E4  2.1E5  1.8E6
Reliability Method

Extrapolation for Low Field MTTF

<table>
<thead>
<tr>
<th>Oxide Field (MV/cm)</th>
<th>Mean Time to Failure (hr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10^{-2}</td>
<td>10^8</td>
</tr>
<tr>
<td>10^0</td>
<td>10^6</td>
</tr>
<tr>
<td>10^2</td>
<td>10^4</td>
</tr>
<tr>
<td>10^4</td>
<td>10^2</td>
</tr>
<tr>
<td>10^6</td>
<td>10^0</td>
</tr>
<tr>
<td>10^8</td>
<td>10^{-2}</td>
</tr>
</tbody>
</table>

Graph showing the relationship between Oxide Field (MV/cm) and Mean Time to Failure (hr).
Power DMOSFET Cross Section

Relevant Internal Resistances

- Increase Mobility
- Reduce $D_{IT}$

**Symbols and Equations:**

- $R_{Channel}$
- $R_{JFET}$
- $R_{Drift}$

**Equation:**

$$R_{Drift} = \frac{d}{q\sqrt{\bar{n}N_D}}$$
Historical Progress of SiC MOS

Improved Clean and Unload

- PMOS-C measured with High-Low Method at 350°C
- $D_{IT} < 2 \times 10^{11}$ cm$^{-2}$eV$^{-1}$ with RCA clean and gentle unloading

$D_{IT} \times 10^{11}$ cm$^{-2}$ eV$^{-1}$

$E - E_V$ (eV)

Historical Progress of SiC MOS

950°C Re-Oxidation Anneal

- PMOS-C measured with High-Low and Conductance at 300°C
- \( D_{IT} < 1E11 \text{ cm}^{-2}\text{eV}^{-1} \) near midgap with 950°C Reox Anneal

Historical Progress of SiC MOS

Reduced $Q_{ox}$ in Reoxidized Samples

- PMOS-C measured at room temperature
- $Q_{ox} = 5 \times 10^{11}$ cm$^{-2}$ with 950°C Reox Anneal (50% reduction)

Historical Progress of SiC MOS

MOSFET Turn-On Remains Poor!
Non-Idealities in the SiC MOS System

Surface Morphology

Increased surface roughness decreases the channel mobility at high fields

Large magnitude of surface roughness may cause discontinuity in the inversion layer
Non-Idealities in the SiC MOS System

Surface Potential Fluctuations

Isolated pools of electrons
But the True Culprit Is... $D_{IT}$

Despite all of the interface improvement in the lower half of the bandgap, the upper half of the bandgap remains relatively unaffected.


Which Interface Traps Matter?

\[ E_c \]

\[ E_i \]

\[ E_F \]

\[ E_v \]

Inversion

\[ D_{IT} \] in the upper half of the band gap is critical to n-channel MOSFET turn-on.

Metal

Ox

Semiconductor

or
First Major Breakthrough

Post Oxidation NO Anneal

Order of magnitude $D_{IT}$ reduction with POA in NO at 1175°C

Reduced Stretch Out of NMOS C-V

Post Oxidation NO Anneal

**ReOx**

**NO**

**Significant stretch-out of CV due to interface traps**

**Minimal stretch-out of CV due to reduced trapping**
Improved NMOSFET C-V with NO Anneal

$C_G - V_G$ with Source, Drain, Body Grounded

- Flat Band @ -6 V
- Turn On @ -1 V
- Fully On @ 2 V
Improved MOSFET Turn-On

Post Oxidation NO Anneal

![Graph showing improved MOSFET turn-on characteristics with post oxidation NO anneal. The graph plots drain current (A) and channel mobility (cm²/Vs) against gate voltage (V). The red and blue lines represent the change in current and mobility respectively.]
Gate Oxide Leakage Characteristic

Dielectric Strength > 10 MV/cm

>90% Yield
Time Dependent Dielectric Breakdown

![Graph showing Mean Time To Failure vs. Oxide Field for NMOS-C, 175°C, and PMOS-C, 175°C. The acceptable MTTF is 100 years. The graph also shows operating fields at 300°C.](image)

- **NMOS-C, 175°C**
- **MOSFET, 175°C**
- **PMOS-C, 175°C**
- **NMOS-C, 300°C**

**Oxide Field (MV/cm)**

**Mean Time To Failure (hr)**

- **Acceptable MTTF:** 100 years
**Improved 1800V MOSFET Performance**

**Post Oxidation NO Anneal**

\[ R_{on,sp} = 8.1 \, \text{m}\Omega \cdot \text{cm}^2 \quad \text{(at } V_{gs} = 15 \, \text{V)} \]

\[ BV = 1800 \, \text{V} \quad \text{(at } V_{gs} = 0 \, \text{V)} \]

Improved 10 kV MOSFET Performance

Post Oxidation NO Anneal

\[ \text{R}_{\text{on,sp}} = 111 \, \text{mΩ} \cdot \text{cm}^2 \]
\[ V_F @ 5A = 3.9 \, \text{V} \]

\[ 10 \, \text{kV} \at \, 11 \, \text{A/cm}^2 \]

\[ BV > 10 \, \text{kV} \]
\[ V_G = 0 \, \text{V} \]

Cooper Plot Perspective for SiC MOS Switches

- Silicon Unipolar Limit
- 4H-SiC Unipolar Limit

- 1998 UMOS
- 1999 DMOS
- 2001 UMOS
- 2001 SIAFET
- 2002 UMOS
- 2001 SEMOS
- 2003 DMOS
- 2004 DMOS
- 2006 IGBT

Graph axes:
- $R_{ON,sp}$ (mΩ cm$^2$
- Blocking Voltage (V)

Legend:
- Blue circles for UMOS
- Green circles for DMOS
- Purple stars for IGBT
- Orange line for Silicon Unipolar Limit
- Orange line for 4H-SiC Unipolar Limit
Future MOS Prospects for SiC

Dealing with the Sub-Oxide Issue

• **Sub-Oxide formed by the conventional thermal oxidation of SiC**
  – Competition between Si and underlying C to oxidize

• **The Sub-Oxide may give rise to 2 major non-idealities in SiC MOS**
  – Interface states ($D_{IT}$) – affects (1) mobility and (2) threshold
  – Fixed oxide charge ($Q_{OX}$) – affects (1) threshold and (2) mobility

• **Sub-Oxide formation may limit the effectiveness of conventional nitridation (NO and N$_2$O) due to in-situ oxidation**
Future MOS Prospects for SiC

Minimizing the Sub-Oxide Formation

• **Ammonia (NH$_3$) annealed oxide**
  – No in-situ oxidation caused by NO or N$_2$O

• **Deposited oxides**
  – No consumption/incorporation of the SiC into the sub-oxide layer

• **Metal Enhanced Oxides (MEO)**
  – Faster oxidation precludes the sub-oxide formed by the competition between Si and C to oxidize
Conductance of Dry Oxide + NO Anneal

Large, Broad Conductance Curves

\[ D_{IT} = 5 \times 10^{11} \text{ eV}^{-1} \text{cm}^2 \]

\[ V_G = V_{FB} \]

\[ \Delta_{US} = 3.5 \text{ kT} \]

\[ E_C - E = 0.2 \text{ eV} \]
Conductance of Dry Oxide + NO Anneal

Stationary Conductance Peaks

\[ V_G = V_{FB} \text{ to } V_{depl} \]
Conductance of Dry Oxide + NH$_3$ Anneal
Smaller, Narrower, Mobile Conductance Peaks

$D_{IT} < 1 \times 10^{11}$ eV$^{-1}$cm$^{-2}$

$\Box_{US} = 1 - 1.5kT$

Increasing $|V_G|$
Improved Channel Mobility

NH$_3$ Anneal Results in Better MOSFET Performance

Field Effect Channel Mobility (cm$^2$/V-s)

Gate Voltage (V)
Limitations of Deposited/NH$_3$ Oxides

- **Poor gate yield**
  - Most likely due to the NH$_3$ etching the exposed gate oxide
  - Majority of devices have gate leakage problems

- **Poor reliability**
  - Non-leaky devices exhibit significantly reduced dielectric strength (~5 MV/cm)
  - MTTF is very low
Metal Enhanced Oxidation (MEO)
Oxidation in the Presence of Alumina

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>SiC Wafer</th>
<th>Alumina</th>
<th>SiC Wafer</th>
<th>SiC Boat</th>
<th>SiC Boat</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to 500</td>
<td>1054</td>
<td>1172</td>
<td>1233</td>
<td>1267</td>
<td>1303</td>
</tr>
<tr>
<td>500 to 1000</td>
<td>803</td>
<td>1076</td>
<td>1129</td>
<td>1175</td>
<td>1235</td>
</tr>
<tr>
<td>1000 to 1500</td>
<td>716</td>
<td>941</td>
<td>1023</td>
<td>1086</td>
<td>1083</td>
</tr>
<tr>
<td>1500 to 2000</td>
<td>650</td>
<td>856</td>
<td>952</td>
<td>990</td>
<td>989</td>
</tr>
<tr>
<td>2000 to 2500</td>
<td>632</td>
<td>825</td>
<td>883</td>
<td>921</td>
<td>907</td>
</tr>
</tbody>
</table>

1000°C Dry O₂ 1 hr

C-V of SiC NO Anealed NMOS-Capacitor

Slight Stretch-Out and Flatband Shift
C-V of SiC MEO NMOS-Capacitor

Almost Ideal C-V is obtained
Conductance of SiC MEO NMOS-Capacitor
Well-Behaved $G_p/w$ Curves
Improved Channel Mobility
MEO Results in Better MOSFET Performance

![Graph showing improved channel mobility with MEO results in better MOSFET performance.](image)

- ReOx
- NO
- MEO

5 μm Epitaxy
Al: 5E15 cm⁻³

- Al: 5E18 cm⁻³, 0.5 μm
Epi: 5 μm, Al: 5E15 cm⁻³
Limitations of MEO Oxides

- **Sodium contamination**
  - Sodium manifests itself as a positive mobile ion in the gate oxide
  - Several volts of threshold shift occur
- **Incompatible with DMOSFET processing**
  - The quality of the interface degrades with any post metallization processes at elevated temperature
  - Forming an ohmic contact to SiC becomes difficult

Summary

SiC MOS technology has matured dramatically within the past decade.

Thermal Dry-Wet Oxides:
- Charge Coupled Devices (Sheppard, Purdue U.)
- CMOS Circuits (Ryu, Purdue U.)
- 9 kV Power IGBT (Zhang, Cree Inc.)

Nitrided Oxides:
- 1200 V Power MOSFET (to be commercialized in 1 year)
- 10 kV Power MOSFET (20 kHz SSPS, Navy)
- DRAM Non-Volatile Memory (Dimitrijev, Griffiths U.)

Next Generation Oxides:
- 600 V Power MOSFET (Cree, Inc.)
- RF Power LDMOSFET (Alok, Philips)