Summary/Agenda

• Overall Process Flow
• Photolithography
• Ion Implantation
• Etch Processes
• Thin Film Deposition
  – Metal Films
  – Dielectric Films
Epitaxial growth, multiple layers of material processing steps, metal contacts and device isolation are integral part of Semiconductor processing steps.
MESFET added to standard HBT process with 1-2 additional masks

PROCESS HIGHLIGHTS:
A) Channel defined by wet etch to etch-stop layer
B) Gate opening defined by dry etch
C) Devices isolated by EM etch after CH etch
PHOTOLITHOGRAPHY & IMAGE REVERSAL

COAT → EXPOSE → DEVELOP
Lithography Requirements

HBT
• Smallest Feature: 0.9 μm

pHEMT
• 0.5 μm and below
Process Sequence

For the definition of metal lines, Plasma Etch Process is used in Silicon Device Fabrication, Lift-Off Technique is used in GaAs Processing

Williams, Modern GaAs Processing Methods p.116
Photolithography Stepper

• Basically a Giant “Camera”
  – Using a stencil (reticle), the camera projects the feature through a lens, which reduces the size of the image by 500%, and onto the wafer surface.
  – This image must be accurately reproduced (shape and dimensions) and aligned to the existing patterns on the wafer

• Critical Components
  – Illumination system
    • Lamp uniformity ≥ 99%
    • 365 nm band pass control (i-Line)
  – Reduction lens
    • Reduction error ≤ 1 ppm @ 20X20 mm field
    • Resolution ≤ 0.50 um
  – Theta Stage
    • Theta (rotation) accuracy and repeatability
    • Scaling (stage magnification)
    • Orthogonality (squareness of stepping)

Sub-90nm “definition” depends not only on the exposure wavelength, but also on advanced optical correction techniques such as “Optical Proximity Correction”, “Phase Shift Mask” etc.
Critical Components (continued)

- **X-Y Stage**
  - Stepping accuracy and repeatability
  - Scaling (stage magnification)
  - Orthogonality (squareness of stepping)

- **Tilt Stage**
  - Focus accuracy and repeatability
  - Tilt accuracy and repeatability
  - Measures and corrects for tilt and focus prior to exposure
    - Can be either intra-field or globally by wafer
Image Reversal

• Metals used for Interconnects and Resistors create processing Problems
  – Gold not easily etched
  – Thin resistor metals have no etch-stop

• Additive Metal Process
  – Image-reverse resist patterned with desired template
  – Metal evaporated onto wafers
  – When the resist is stripped off, the unwanted metal is removed from the wafer
• After first exposure, subject to ammonia vapor. Amine diffuses through the resist and reacts with the carboxylic acid byproduct in the exposed area, removing the dissolution enhancer.

• A second flood exposure by UV at high dose is performed, making the previously unexposed area soluble.

• Follow by standard develop, etc.

• Advantages: resolution equal to the positive resist image, good CD control and depth of focus
  – Dark field masks are preferred over light field masks (particles), positive photo resist is preferred because of resolution
Typical Resist Coat Process

For Lift-off:

Expose ⇒ Image Reverse ⇒ Develop ⇒ Descum ⇒ Deposit Metal

⇒ “Lift-off”

From: S. Wolff and R.N. Tauber, Silicon Processing for the VLSI Era (Vol. 1) p. 429
Metal-2 prior to Lift Off

Critical Gap for Clean lift-off

Au
Resist
Substrate
Au
• **Critical Dimensions**
  
  – Line width measurement
    
    • Optical slit scan technique
    
    • In-line SEM
  
  – Scanning electron microscope (SEM) is used for the CD measurements
  
  – Features typically magnified by 35,000 X
  
  – Understanding the process is critical for successful use of SEM tool

• **Overlay Measurements**
  
  – Optical microscope tools (KLA and IVS) are used for the overlay measurements
  
  – Process relies heavily on pattern recognition imagery and program set-up
  
  – Parameters affecting accurate measurements
    
    • Resist thickness
    
    • Substrate reflectivity and thickness
    
    • Topology
ION IMPLANTATION FOR
DEVICE ISOLATION

- Im planted ions
- Crystal Lattice
- Surface Modified Layer
Why Do We Need Isolation Implant?

- Epi layers are conductive
- Need to isolate the active areas from each other
- Non-reactive ions are implanted and damage crystal structure
- Implanted areas become non-conductive (insulating)
Eaton8250 - How Does Implant Work?

(1) Ion Source: Generates Ion Beam
(2) Ion Acceleration
(3) Impinge on Wafer
Parameters in Implantation

• Ion Implantation “with no sputter component”, can be described statistically and modeled as a “Gaussian” distribution.

\[
N(x) = N_p \exp\left(-\frac{(x - R_p)^2}{2\Delta R_p^2}\right)
\]

Where \(N_p\) is the peak impurity/damage concentration, \(R_p\) is projection range (function of Ion energy), \(\Delta R_p\) is lateral straggle (half width @ half maximum).

• “Dose” is defined as the total number of ions implanted per cm\(^2\)

\[
D = \int_{-\infty}^{\infty} N(x) dx
\]

• In terms of Machine Parameters:

\[
D = \left[\frac{\text{ion beam current in amps}}{\text{implant area}}\right] \times \left[\frac{\text{implant time}}{\text{implant area}}\right]
\]

Where \(q\) is the ion beam current in amps, \(\text{implant area}\) is the area over which the implantation occurs, and \(\text{implant time}\) is the duration of the implantation process.
Isolation Implant: Where?

Photo resist - protects active area

Damage Zone - Insulating

- InGaAs
- GaAs
- AlGaAs Buffer
- GaAs Buffer
- SI GaAs Substrate
- AlGaAs Emitter
- Second Collector
- First Collector
- Protection nitride
- ~x,000A
- ~x,000A
- Damage Zone - Insulating
Isolation Implant: How?

- Proton Isolation was Used Earlier
- Helium is Used for Better Reliability
- Boron even better for surface isolation
  - Implant profile is \( \sim \) Gaussian (\( \rightarrow \))
  - Need to isolate shallow and deep
    - **High** KeV implant (\( \sim 400 \text{keV} \))
      - must reach Sub-collector
    - **Low** KeV implant (\( \sim 200 \text{keV} \))
      - must isolate the Surface
  - **Adding** peaks together gives approximately a flat profile
  - Avoid “Channeling” effect by tilting the wafer to the incoming ions.
Implant Isolation in FET Type Circuits

- Device isolation can be achieved by Ion Implantation without mesa etching (leads to “planar” surface).

- Gate metal does not contact the doped, conducting area on mesa side wall – improved leakage and reliability

- Boron is a Good Ion

  - Low mass, need high dose, high mass causes excessive damage
  - Good isolation at the Substrate-Epi interface reduces “Back-gating” effect
  - Low dose, high throughput
  - No annealing needed, hopping conduction not an issue

The Stopping and Range of Ions in Matter (SRIM) is an excellent software package, developed by Dr. James Ziegler, that simulates the ion implantation process and is available online (http://www.srim.org).
DRY & WET ETCH PROCESSES

**Plasma dry etch**
- Chemical assisted Ion beam etch
- Reactive Ion Etch

**Wet Etch**
- Chemical Etch
  (Isotropic Etch)

![Plasma dry etch](image)

![Wet Etch](image)
Etch Processes

HBT

• Emitter: InGaAs Etch + GaAs Dry Etch
• Base Pedestal: Wet/Dry Etch
• Base Contact: Nitride Etch + AlGaAs or InGaP Dry Etch
• Collector: Wet Etch

FET

• Channel: Wet Etch
• Gate Recess: Wet Etch

Interconnects

• Inter layer Dielectric (Polyimide): Dry Etch
• Nitride cap or Passivation Nitride: Dry Etch
Etch Profile & Selectivity

\[ L_T = \frac{\text{Horizontal Etch Rate}}{\text{Vertical Etch Rate}} \]

\[ A \ (\text{Anisotropy}) = 1 - L_T \]

- Selectivity w.r.t. mask is needed to maintain feature size
- Selectivity is also needed w.r.t. the underlying substrate to prevent loss of previously processed circuit, and allow adequate over-etch.

S. Wolff and R.N. Tauber *Silicon Processing for the VLSI Era*, Vol. 1

Mask etching as substrate is etching
## Wet or Dry Etch?

<table>
<thead>
<tr>
<th>Dry Etch</th>
<th>Wet Etch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complex tools</td>
<td>Simpler tools</td>
</tr>
<tr>
<td>High tool cost</td>
<td>Low tool cost</td>
</tr>
<tr>
<td>Low material cost</td>
<td>High chemical cost</td>
</tr>
<tr>
<td>Low environmental impact</td>
<td>High environmental impact</td>
</tr>
<tr>
<td>Control of etch profile</td>
<td>No control of profile</td>
</tr>
<tr>
<td>Sub-micron geometries</td>
<td>Micron geometries</td>
</tr>
<tr>
<td>Good dimension control</td>
<td>Poor dimension control</td>
</tr>
<tr>
<td>Good selectivity</td>
<td>Typically poor selectivity</td>
</tr>
<tr>
<td>Good uniformity</td>
<td>Poor uniformity</td>
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</table>
## Wet Etch Selectivity Table

<table>
<thead>
<tr>
<th>Etchant</th>
<th>GaAs</th>
<th>InP</th>
<th>InGaAs</th>
<th>InGaAsP</th>
<th>GaInP</th>
<th>GaAsP</th>
<th>AlGaP</th>
<th>AlGaAs</th>
<th>AlInP</th>
<th>InAlAs</th>
<th>InGaAlAs</th>
<th>SiO₂</th>
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<tbody>
<tr>
<td>HCl : H₃PO₄</td>
<td>S</td>
<td>E</td>
<td>S</td>
<td>S</td>
<td>S</td>
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<tr>
<td>H₃PO₄ : H₂O₂ : H₂O</td>
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<tr>
<td>H₂SO₄ : H₂O₂ : H₂O</td>
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<tr>
<td>C₆H₃O₇ : H₂O₂</td>
<td>CD</td>
<td>S</td>
<td>CD</td>
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<tr>
<td>HCl : HNO₃ : H₂O</td>
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<td>HCl : H₂O₂ : H₂O</td>
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<tr>
<td>HCl : H₂O</td>
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<td></td>
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<tr>
<td>BHF : H₂O</td>
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<td>E</td>
</tr>
</tbody>
</table>

### Legend

- **Etches**
- **Selective/ Stops**
- **Composition Dependent**
- **No Data**

**From: Umd.edu Web site**

**More detailed reference: Clawson Guide to Wet Etching, A.R. Clawson, UCSD**
Wet Etch Anisotropy in GaAs

GaAs: Zincblende Structure

\[ \text{ER}((111)\text{As}) > \text{ER}((100)) > \text{ER}((111)\text{Ga}) \]

View of GaAs lattice from different directions

Williams, *Modern GaAs Processing Methods*, p. 24
Etch Depths

Channel Etch

Emitter

Mesa Etch

Base Contact

Collector Pedestal Contact

InGaAs GaAs+ InGaP

GaAs

InGaAs+ GaAs+ InGaP

InGaP+ GaAs

InGaP+BC Deposition

Base Collector

Cap layer

channel

Emitter

Base

Collector

Buffer

Substrate

N+ InGaAs (y = 60%)

Te

N+ InGaAs (y = 0, 60%)

Te

N+ GaAs

Si

N InGaP

Si

N Channel GaAs

Si

P+ GaAs

C

N+ GaAs

Si

N+ GaAs Collector

Si

AlGaAs Undoped

A

GaAs Undoped

A

Si GaAs Substrate
Mesa Etch (Wet + Dry)

• Though Dry etch process provides better control of the Critical Dimensions, in HBT, it is desirable to have the mesa defined by the combination of dry and wet etch, as the wet etch reduces Cbc.
**HBT – Emitter & Base Definition Etches**

- **GaAs/AlGaAs Etch Stop on AlGaAs**
  - Step 1 Bulk InGaAs/GaAs etch, terminate by time
  - Step 2 Selective etch
    - Use SiCl₄
    - Introduce SF₆, reduce r.f. power level
    - RF power low – low bias
    - Pressure low - lower etch rate

- **AlGaAs/GaAs Etch Stop on GaAs**
  - No selectivity of AlGaAs to GaAs
  - Need optical emission endpoint
    - GaCl* @ 417 nm
    - BCl3 low background emission 400-420nm
  - For InGaP, use InCl* signal from the layer that is being etched or use AsCl* from the underlayer.
• Significant overetch into the base layer will lead to contact metal spiking into the Base and will lead to increased Vce-offset in the HBT Devices.

• Uncontrolled Etch of AlGaAs or InGaP Ledge will punch-through the base GaAs, leading to increased B-C leakage and/or long-term reliability effects.
THIN FILM DEPOSITION

CHEMICAL VAPOR DEPOSITION (CVD)
• APCVD – Atmospheric Pressure ...
• LPCVD – Low Pressure ...
• PECVD – Plasma Enhanced ...
• HDPECVD – High Density ...

PHYSICAL VAPOR DEPOSITION (CVD)
• E-Beam Evaporation
• Thermal Evaporation
• DC Sputtering
• RF Sputtering

DIELECTRICS

METALS
E-Beam evaporated metals are used to make:
- Emitter, Base, Collector contacts of HBT
- Schottky Diode (Anode contact)
- Schottky Gate Contact Metallization in MESFET/HEMT
- Interconnects: Metal-1, Metal-2, Metal-3 …
  - Inductors, capacitors, transmission lines

Sputtered metals are used to make:
- Thin Film Resistors (TFR), TaN
- Seed layer for Gold plating, TiW Barrier layer
Evaporation Advantages

Advantages

✓ High purity films can be deposited
✓ Source material may be a solid in any form
✓ Line of sight deposition (good for lift-off)
✓ Deposition monitoring and control relatively good
✓ Least expensive form of PVD

✗ Careful design of the dome and distance from source to wafer are critical to prevent “Gate-Walking” in pHEMT/MESFET devices

For Gate position symmetrical at wafer edges, throw distance in evaporator has to be large
Sputtering

- **Advantages**
  - Elements, alloys and compounds can be deposited
  - Good sidewall (conformal) coverage
  - Stable, long lived target/source

- **Disadvantages**
  - Sputter rates are low compared to evaporation
  - Sputter targets are expensive
  - Material utilization is somewhat poor
  - Radiation and ion bombardment can damage substrate
  - Not good for lift-off processes
Evaporation: Variables & Responses

• Factors/Input Variables
  – Deposition Rate
  – Ramp Time and Power
  – Base Pressure
  – Refractory Metal Liners
  – Melt Weight
    - Shaper
    - Crystal Life
    - Cleanliness
    - Vent Speed
    - Pre-deposition Clean

• Responses
  – Thickness Uniformity
  – Film Density/Texture
  – Adhesion
  – Particle Count/Nodules/Haze
Schottky Contact Metal

Metal-Semiconductor Band-Diagram

Planar Diode

On Conducting Substrate

Commonly used contact metals

Typical I-V of Schottky Diode

Ghandhi, VLSI Fabrication Principles Si and GaAs
Ohmic Metallization

- **To n-Type GaAs**
  - 750Å AuGe, x Å Ni, 800Å Au, y Å Ti
  - Ohmic contacts allow current to flow into and out of the substrate with linear resistance
  - AuGe has proven best for low Rc
  - The ratio of AuGe to Ni is crucial to achieving low Rc after alloy
  - Exact total thickness is less critical
  - After ohmic deposition, lots go to alloy

- **In the case of n-type In doped GaAs**
  - Ti/Pt system will give Ohmic contact since the Fermi level is close to the conduction band (due to In)
1) The emitter is InGaAs, very low band gap
2) Base is heavily doped p+ GaAs, Pt is used as contact metal
3) Au/Ge/Ni alloyed contact is used for collector, low contact resistance is due to NiAs(Ge) in contact with heavily Ge doped GaAs

Ref: Murakami et. al Interfaces between Ohmic Contacts and GaAs IBM esearch Report Materials Science (1989)
• During alloy the wafers are raised to 360-380° C which causes the metals in the stack to mix and diffuse into the crystal structure
  
  – AuGe is used for doping the GaAs which provides an ohmic contact
  
  – Ni acts as a “wetting” agent for AuGe, helping it diffuse into the GaAs
  
  – Gold provides low resistance and better contact to M1

• Contact resistance drops dramatically after alloy

• Transmission line measurement (TLM) measurements and visual inspection after alloy
  
  – Over alloy-rough texture
  
  – Under-alloy-non-linear TLM
  
  – Leopard spots, nodules or blisters could show up after alloy
Particle Control in Evaporators

- Capacitors tend to have relatively large areas on surface of wafers.
- This increases the probability that a particle will land on a capacitor.
- Evaporators must be designed for Low Particle Counts

- **System Cleanliness**
  PMs, flaking, melt, pockets, pre-treatment of surfaces

- **Process Optimization**
  - Ramp rate
  - Soak power (power level just before shutter opens), etc.
  - Source materials
  - Liners
  - Vent and pump speed

Particle monitoring from each process run is vital to ensure the quality of the MIM capacitors
Dielectric Films in GaAs Processing

Typical Dielectric Films used in Compound Semiconductor Processing are:

- Silicon Nitride (Plasma Enhanced CVD)
  - Implant anneal cap layer
  - Device passivation (Low Stress thin film)
  - MIM capacitors (High Density thin film)
  - Inter level Dielectrics (Between 2 interconnect metals)
  - Overcoat (Passivation/Moisture barrier)

- Polymers (Spin-on Coating)
  - Polyimide (Inter level Dielectrics)
  - Poly Benzoxazole (Scratch protection layer on SiNx)
  - BCB (Cyclotene*)

*Trademark of The Dow Chemical Company ("Dow") or an affiliated company of Dow
Where SiNx is used?

Silicon Nitride is the most commonly used “Dielectric Material” in Compound Semiconductor Manufacturing.
- Multiple layer (7) deposition prevents propagation of pinholes
- Dual frequency to control stress and increase nitride density
- High throughput

From: Novellus Concept II Brochure
PECVD-Plasma Enhanced Chemical Vapor Deposition

**Independent Film Stress Control**

- **Stress (E9 dynes/cm²)**
- **Low Frequency Power (Percent)**

Source: Customer production data.

*LF power is used to control stress*
Advantages of Novellus PECVD

- Very conformal Coating
- Low pin hole density
- Low Hydrogen content
- Independent stress control
- Low particle levels
- Reproducible process as a result of automatic cleaning

From: Novellus Concept II Brochure
Summary

• From Optoelectronic to Power Devices based on Compound Semiconductors, standard fabrication processes involve dielectric deposition, thin film metallization, ion implantation and thermal annealing steps.

• Though the Epitaxy is the key to the fundamental performance of the compound semiconductor devices, feature sizes and unit process modules and their controls are paramount to achieve high yield and quality.

• Understanding the device-process interactions, Design of Experiments to establish optimized process steps and establishing statistical process control are vital in high volume manufacturing.

• Planarization techniques, low cost alternative metals (to Au), High-k dielectric capacitor materials, coatings as moisture barriers (hermetic seal) are beneficial.