Device Processing in III-V Manufacturing: Backside Wafer Processing

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CS Mantech 2010 Workshop:
Overview of Device Processing in III-V Manufacturing
Why, why, why!

**Electrical:**


**Thermal:**


*Process Considerations for Manufacturing 50 µm Thinned III-V Wafers*, G. Cobb, H. Isom, C. Sellers, V. Williams, CS MANTECH Conference, May 14-17, 2007, Austin, Texas, USA

**Functional:**


**Packaging:**


**Density:**

**Product performance:**
Figure 1. Vertical GaAs Monolithic Shunt Diode with Single Via Hole

**Electrical**

**Functional**

**Packaging**

Figure 3: Illustration of an ICIC inside WLP.
Process Flow - High Level

- Mount
- Thin
- Via
- Metal
- Demount
- Dice
- Bond (permanent or temporary)
- Grind
- Photo/Etch
- Dep/Photo/Etch (or liftoff)
- Debond
Process Flow - High Level

Mount

Thin

Via

Metal

Demount

Dice

Bond (permanent or temporary)

Grind

Photo/Etch

Dep/Photo/Etch (or liftoff)

Debond
Aligned wafer bonding - overview

Slide courtesy of EV Group
Types of Bonding

NOTES
1. May be mechanically or optically aligned. Bonding process will effect final alignment results.
2. May be used for permanent or temporary bonding.
3. Inclues adhesive bonding.
4. TLP – Transient Liquid Phase.
5. Also called direct bonding or molecular bonding. Has strict requirements for flatness, surface finish, and contamination.
6. Also called metal diffusion.
7. Requires special bond chamber.
# Bonding Process Requirements

<table>
<thead>
<tr>
<th></th>
<th>No Intermediate Layer</th>
<th>Intermediate Layer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Surface Roughness</strong></td>
<td>&lt; 20 nm</td>
<td>&lt; 0.5nm</td>
</tr>
<tr>
<td><strong>Layer Thickness</strong></td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td><strong>Process Temperature</strong></td>
<td>400 - 500 C</td>
<td>1000 C (anneal)</td>
</tr>
<tr>
<td><strong>Cleanroom Environment (FS209E)</strong></td>
<td>100</td>
<td>10 or 1</td>
</tr>
<tr>
<td><strong>Sensitivity to Particles</strong></td>
<td>Medium High High Low Medium Medium Medium Low Low Low</td>
<td></td>
</tr>
<tr>
<td><strong>Sensitivity to Surface Contamination</strong></td>
<td>Medium Very High Very High Medium High High Low Low Low</td>
<td></td>
</tr>
<tr>
<td><strong>Na present</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Cycle Time (minutes)</strong></td>
<td>45 - 90</td>
<td>Bond ~ 1 Anklel - hrs</td>
</tr>
</tbody>
</table>

*Slide courtesy of EV Group*
## Bonding Process Variables

### Incoming
- **1. Wafer**
  - a. Size
    - i. Diameter
    - ii. Thickness
  - b. Material
    - i. CTE
  - c. Bow & Warp
  - d. TTV
  - e. Vacuum integrity

### In Chamber
- **1. Standard Bond Chamber**
  - a. Time
  - b. Temperature
  - c. Force
  - d. Atmosphere
  - e. Wafer to wafer spacing (flags)
  - f. Bow Pin
  - g. Voltage / current

### Outgoing
- **1. Wafer**
  - a. Bow & warp
  - b. TTV
  - c. Breakage

### Contact Layers
- **1. Alignment**
- **2. Spacing (gap between wafers)**

### Color Code
- Items in RED are controlled by upstream process
- Items in Green are controlled by alignment system
- Items in BLACK are controlled by bond chamber
- Items in BLUE are output variables

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### Notes
- [1] Can the wafer be handled by backside vacuum or will edge handling or other special handling be required?
- [2] Translates to pressure based on bond contact area
- [3] Vacuum, forming gas, inert gas; no toxics or corrosive gasses.
Types of Alignment for Bonding

- Mechanical
  - Same Size Substrates
  - Different Size Substrates
    - Backside (Front to Back)
      - Direct (Transmission)
        - InfraRed
        - Visible Light
      - Indirect (Reflection)
        - Visible Light
  - Optical
    - Face to Face (Front to Front)
      - Direct (Transmission)
        - InfraRed
        - Visible Light
      - Indirect (Reflection)
        - Visible Light
Optical bond alignment for the EVG® 500 series

Optical bond alignment and wafer bonding are separated

Bond aligner:
Wafers are aligned and fixed to a bond chuck

Wafer bonder:
Wafers are bonded (pressure, temperature, vacuum)

Bond chuck transfer
Coating Methods

Spin Coating
Wafers
• Blank wafers
• Wafers with little to no Topography
• Square substrates (without topography)
• Bump wafers

Markets – All:
• Standard semiconductor
• MEMS
• Power devices
• Optical systems
• Packaging
Coating Methods

OmniSpray® Coating

Substrates and wafers with
- High topography
- Trenches or through etched holes
- Wafer pieces
- Multiple substrates on carrier

Markets:
- MEMS
- MOEMS
- BioMEMS
- Compound semiconductor
- Packaging

Slide courtesy of EV Group
OmniSpray® Coating Application

BCB Coating tests on 8" Si-Wafer

1. 10µm layer with BCB 4026-46 Spin coating (area dispense)
2. 5µm layer with BCB 4024-40 Spin coating (area dispense)
3. 10 µm layer with BCB 4026-46 Spray coating
4. 5µm layer with BCB 4024-40 Spray coating

Slide courtesy of EV Group
Process Flow - High Level

Mount

Thin

Via

Metal

Demount

Dice

Bond (permanent or temporary)

Grind

Photo/Etch

Dep/Photo/Etch (or liftoff)

Debond
CS-Specific Considerations

CS are very brittle after backgrind

- Standard backgrind tape provides insufficient support for subsequent wafer handling/processing when thinning below 200um
  - Support carriers generally required
  - Bonding process becomes critical to ensure 100% enclosure & support of device wafer by carrier wafer (minimize grind damage)

Backgrind wheel selection

- To prevent unwanted damage of GaAs, proper wheel selection critical to provide efficient cutting with minimal force

Post-grind etching / polishing

- Required to provide stress relief of ground wafer & etch through grind-induced damage
  - Chemical selection important to provide isotropic etch
  - CMP an alternative to wet chemical etch
- Etch / polish also improves surface quality of ground material
Backgrind Process

Typical method of grinding is top-down in-feed of grind wheel to rotating vacuum grind chuck

- Others methods such as creep-feed (wafer fed laterally through grind wheel) exist as well

Wafer held in place by vacuum chuck. Removal occurs via feed of grind wheel assembly through wafer with concurrently rotating grind wheel and chuck

Two grinds / wheels:

- Coarse grind: bulk removal of material at high feed rates using harder wheel
- Fine grind: final material removal at slow feed rates using softer wheel
  - Removes damage incurred during coarse grind & provides more polished surface of wafer
  - Grind removal amount balanced with feed rates to reduce throughput considerations
“Thickness” or removal controlled by in-situ probe(s) during grind. Allows for support/bond/device stack thickness to be targeted to a specific value (prior knowledge of support & bond layers is required), or a pre-determined thickness of material to be removed from the device wafer.
Backgrind process control parameters

• **Primary**
  - Grind wheel rotational speed
  - Vacuum chuck rotational speed
  - Grind wheel feed rates

• **Secondary**
  - Cutting $H_2O$ flow rates & application
  - Chuck cleanliness (planar chuck surface required to reduce grind defects)
  - Chuck vacuum capability (entire wafer required to be held firmly in place during grind to reduce wafer fluttering & damage)
  - Grind wheel angles & direction (can be adjusted to achieve optimal TTV & minimize wafer damage)
Grind wheel selection
Critical to uniform thickness targeting & surface finish

Resinoid wheels best suited for GaAs backgrind

- Key grind wheel considerations:
  - Diamond mesh size
  - Diamond concentration
  - Bond material hardness
  - Bond material porosity & distribution

Selected based on above criteria balances self-dressing needs, wheel lifespan, and device wafer surface finish
Backgrind-initiated defects

• Star cracks – caused by debris on the chuck or embedded debris in the bonding layer

• Edge chipping – caused by poor edge bonding resulting in unbonded material becoming over-ground and breaking off

• Over-grind – usually initiated by non-uniform bonding layer thickness or poor bond allowing for water encroachment between the device & support wafers. Over-grind results in a region much thinner than surrounding areas and appears to have a burnished appearance

• Chatter & Gouging – caused by grind debris or low-hanging diamonds in the wheel that create deep gouges in the wafer surface

• Cross-hatching – caused by non-uniform grind tooth wear, leading to grind marks that run counter to the majority
Backgrind-initiated defects

Edge Chipping

Chatter / Gouging
Post-grind Cleaning

Post-grind cleaning is required to remove residual grind debris from wafer surfaces and prevent contamination of downstream tools.

Many grind tools utilize some form of in-situ cleaning prior to wafer exit:

- Spin/rinse stations
- Backside brush scrubbing

Occasionally, in-situ cleaning is insufficient, and additional cleaning methods are required:

- Brush scrubbing tools provide effective cleaning of grind debris.
Post-Grind Etch/Polish

Post-backgrind wet chemical etch and/or polishing is required on GaAs material to relieve grind-induced stress and reduce roughness of surfaces

• Wet chemical relief etch chemistries need to be tailored to remove desired amount of material in uniform fashion. Typical chemicals can include:
  ➢ Hydrogen peroxide
  ➢ Ammonium hydroxide
  ➢ Phosphoric acid

• Isotropic etching is desired so as to minimize decoration of grind defects. Tool selection can be critical to allow for well-controlled etching

• CMP can be used as an alternative to wet chemical post-grind processing
Post-Grind Etch/Polish

Post-grind etching can expose & highlight subsurface grind damage depending on chemistry

- Damage can become visible to naked eye
Process Flow - High Level

Mount

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Via

Metal

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Bond (permanent or temporary)

Grind

Photo/Etch

Dep/Photo/Etch (or liftoff)

Debond
IR alignment

- Topside objectives
- Photoresist
- Background device wafer
- Cap wafer
- Alignment keys
- Bottom IR illumination
Backside alignment

- Photoresist
- Background device wafer
- Clear carrier wafer
- Alignment keys
- Bottom objectives
Example of IR alignment features

Mask

Aligned mask and wafer
Example of backside alignment features

Mask

Digitized image of mask

Wafer

Aligned mask and wafer
Process Flow - High Level

- Mount
- Thin
- Via
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- Bond (permanent or temporary)
- Grind
- Photo/Etch
- Dep/Photo/Etch (or liftoff)
- Debond
Process Requirements

Good Electrical Performance

- Etched Via Easily Metalized
  - Feature Profile Control
  - Good CD Control
  - Smooth Feature Sidewalls
  - No Post-Etch Residues
- Selective to Underlying Metal

Short Process time

- Fast / Uniform GaAs Etch Process
- Resist Etch Mask

Robust Process

- Tolerant of Upstream Variations
Via Profile Control

Vertical Etch Profile

Sloped Etch Profile

Sloped PR

Slide courtesy of Plasma-Therm LLC
Via Profile Control Vertical

Benefits:

• Good CD Control
• Process Reproducibility

Issues:

• More Difficult to Metalize
• Sidewall Passivation Removal
Via Profile Control
Sloped

Eroding a Sloped Resist Etches a Sloped Via Profile
Via Profile Control
Sloped

Benefits:

• Good CD Control at Front Side
• Process Reproducibility

Issues:

• Profile Highly Dependent on Initial PR Profile
• Roughened Sidewalls
• Sidewall Passivation Removal
• Discontinuous Slope
Via Profile Control
Sloped – Resist Erosion

Several Key Factors Combine for Effective Profile Control

• Initial Photoresist Profile

• Process Conditions
  • Selectivity (GaAs : PR)
  • Chemistry
  • RF Power Levels (Bias)
  • Temperature
Backside Via Etch Performance
Plasma Etch Chemistry

GaAs Via Etch

GaAs + 3 Cl₂ → GaCl₃ + AsCl₃

Typical Process

• Descum
• Breakthrough (highly physical)
• Cl₂ based processes: Cl₂ / BCl₃
  Cl₂ / Ar
Backside Via Etch Performance
Plasma Etch Chemistry

Conventional GaAs via etching involves the use of a chlorine (Cl\textsubscript{2}) based process chemistry.

Additive gases like BCl\textsubscript{3}, Ar, or CH\textsubscript{4} are incorporated for profile or selectivity control.

- Cl\textsubscript{2}/BCl\textsubscript{3} chemistry in a 4:1 or 5:1 gas ratio is a proven production worthy process on the Plasma-Therm Versaline yielding high etch rates and selectivities.

<table>
<thead>
<tr>
<th>Chemistry</th>
<th>Cl\textsubscript{2} only</th>
<th>Cl\textsubscript{2} and BCl\textsubscript{3}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etch Rate</td>
<td>5 µm/min</td>
<td>9 µm/min</td>
</tr>
</tbody>
</table>
Backside Via Etch Performance
Aspect Ratio Dependent Etching

![Graph showing the relationship between aspect ratio and average etch rate. The graph plots Aspect Ratio (etch depth/feature size) on the x-axis and Average Etch Rate (microns/min) on the y-axis. The data points are connected by a curve, indicating a decrease in etch rate as the aspect ratio increases.]

Slide courtesy of Plasma-Therm LLC
Backside Via Etch Performance
Pillar Elimination

Pillars and grassing are detrimental to a backside via process.

Cause:

• Upstream processes:
  • Grinding
  • Mounting
  • Photolithography
  • Material defects
  • Plasma etch process

Solution:

• Plasma etch processing
  • Utilizing a Breakthrough step: a physically driven etch initiation step.
  • Utilizing an optimized, chemically driven main etch step
Manufacturability
ICP Based Via Etch Process

Inductively Coupled Plasma (ICP) GaAs Via Etch Process

Independent Control RF Bias / Density
- GaAs Etch Rate vs. GaAs : Resist Selectivity
- Via Profile Control

High Density Plasma
- High Etch Rate for High Throughput

High Conductance Design
- Low Pressure Operation
- Excellent Within Wafer Uniformity
Manufacturability
Controlled ICP Source Heating

Controlled ICP Source Heating

• Process Stability
• Reduced Maintenance
• Constant Chamber Conditions
Seed dep and plate

Plating is remarkably insensitive to via profile (however this profile isn’t considered “ideal”)

This image is the author’s alone and does not represent typical processing by any of his friends and colleagues (except the great job plating).
Process Flow - High Level

Mount

Thin

Via

Metal

Demount

Dice

Bond (permanent or temporary)
Grind
Photo/Etch
Dep/Photo/Etch

Debond
DeBonding – Process Overview

- **DeBonding**
  - wedge-off
  - slide-off
  - UV-debond

- **Handling**
  - Slide courtesy of EV Group
  - ThinWafer Cassette
  - FilmFrame Cassette
  - Coin Stack Wafer-Canister
  - Single Wafer Carrier

- **Cleaning**
  - Megasonic
  - DI-Water
  - Solvent
  - Diluted Chemistry
  - Brush Scrubber
  - High Pressure

- **Handling**
  - Output Format

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Page 46  Timothy J Whetten
DeBonding – Process Flow

**EVG850DB**
Brewer Adhesive, FilmFrame Output

1. **Adhesive Tape pre cut**
2. **Film Frame**
3. **Waferstack**
4. **Debond Process slide of**
5. **Cleaning Device Wafer**
6. **FilmFrame Mounting**
7. **Cleaning Carrier Wafer**
8. **Device Wafer on FilmFrame**
9. **Carrier Wafer**
Things to worry about
(in case you were sleeping too well)

Wafer breakage
Thin wafer handling
Film Stress
Adhesion
Corrosion
Interaction with solder
Eliminating Edge Chipping

Edge-trimming process prior bonding

- Enables of using SEMI-standard carrier wafer
- Rectangular wafer edge, resulting in higher die strength (as reported per Philips, Netherlands)
- Wafer is slightly smaller after thinning, enabling full support (no resulting sharp wafer-edge)
- Minimized contamination of grinding-wheel
Eliminating Edge Chipping

Investigation on different potential approaches has been realized;

After temporary bonding + thinning step, edge defects have been statistically characterized.

Edge-trimming of device wafer prior bonding is showing significant less defects compared to other approaches.

Courtesy of Dongshun Bai - Brewer Science;
to be presented at ISTC/CSTIC 2009; “Edge Protection of Temporarily Bonded Wafers during Backgrinding”
Backside Processing plus Wafer Scale Packaging

Photograph of the first GaAs Wafer Scale Package products on the market in the 0402 form factor (1mm x 0.5mm x 0.3mm) next to a standard 0402 inductor
Backside Processing plus Wafer Scale Packaging

Henrik Morkner, “GaAs-Based Surface Mount Wafer Scale Package MMICs for DC to 45 GHz Applications”
http://avagotechwireless.com/collateral/AV02-2103EN.pdf

Simplified assembly process

Typical assembly processes

- MMIC Wafer
- Die Singulation
- Die Attach Assembly
- Wire bond Assembly
- Packaging Assembly
- Packaging Singulation

Figure 5a. Typical plastic package assembly process

- MMIC Wafer
- Bonded with Cap Wafer
- Singulation

Figure 5b. WSP equivalent process
Reduced parasitics

Figure 6. Typical parasitics in other SMT technologies
Process Flow - Examples

Temporary Mount

Thin

Via

Metal

Demount

Dice

Temporary Mount

Thin

Via

Metal

Demount

Dice

Permanent Mount

Thin

Via

Metal

Thin

Dice

Dice

Dice