Wafer-Level Packaging and Wafer-Scale Assembly Technologies

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Agenda

• Overview
  – Technology description
  – Benefits

• 2-Layer WLP/WSA
  – Process description
  – Examples

• Interconnects & Transitions

• Package Performance

• Multi-Layer WLP/WSA
  – Process description
  – Examples

• Higher Order Integration
What is Wafer-Level-Packaging?

Wafer-Level Packaging (WLP)
AKA: Micro Packaging
AKA: Wafer-Scale Assembly (WSA)

- Add inter-cavity interconnects and cavity ring
- Stack and bond multiple wafers, then dice
- Forms a hermetically packaged 3-D integrated circuit
- Enables integration of different MMIC technologies

WLP provides low cost, high volume, hermetic packaging
Advanced Capabilities for Next-Generation Systems

- Next-generation system needs performance superiority & affordability

- WLP ⇒ performance superiority
  - Advanced integration
    - best semiconductor technology for the function
  - Ultra-compact, light weight packaging
    - size & weight savings
  - High functional density & low loss interconnects
    - Superior circuit performance
  - Hermetic MMIC packaging
    - Enhanced circuit reliability

- WLP ⇒ Affordability
  - Batch fabrication processes
    - Low cost, high volume
  - Fully compatible with NGAS MMIC production processes
    - Existing & proven MMIC technologies
    - Next-generation MMIC technologies
  - Reduce higher order assembly cost, relax module assembly requirement
WLP Benefits

- **Superiority**
  - Hermetic compact MMIC packaging
  - Performance enabler
    - High functional density
    - Superior circuit performance

- **Affordability**
  - Batch fabrication processes, low cost, high volume
  - Reduce higher order assembly cost, relax module assembly requirement

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<th>Integrated Microwave Assembly (IMA)</th>
<th>Wafer-Level-Package (WLP)</th>
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<tr>
<td><strong>Size reduction</strong></td>
<td>1</td>
<td>1,000X</td>
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<tr>
<td><strong>Weight reduction</strong></td>
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<td>1,000X</td>
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<td><strong>Cost reduction</strong></td>
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<td>10-100X</td>
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Heterogeneous Integration using WLP

Combine multiple MMIC wafers by wafer bonding technology

Tri-layer WLP TR Module
X-band operation
Mass: <15mg
Size: 2.5mm x 2mm x 0.46mm
WLP content: 3 bit PS, LNA, PA

WLP offers superiority in performance and affordability in cost
Integrated Microwave Assembly Packaging

GaAs

InP

GaN

CMOS

IMA
Wafer-Level Integration Benefits

- Hermetic
- Ultra-light weight, ultra-compact
- Low cost, high volume
- Performance enhancement

**IMAs**
- Weight: g to >1000g
- Size: cm x cm x cm
- Assembly: serial, manual

**Wafer-Level Integrated Package**
- Weight: < 50 mg
- Size: mm x mm x mm
- Assembly: mass parallel, wafer scale
Integration Using Wafer-Level Packaging

- WLP is assembled using a low temperature wafer bonding process
- WLP technology is fully compatible with NGAS MMIC production processes

Low temperature wafer bonding process is key to MMIC compatible, robust WLP
2-LAYER WLP
2-Layer WLP

- Wafers are individually processed prior to bonding
  - No changes to standard MMIC processes

- ICIC = Intra-Cavity InterConnections

- BICIC = Backside ICIC

**2-layer Bonding Process Flow**

**2-Layer WLP is constructed by bonding 2 individually processed wafers**
WLP Demonstrations

- WLP is fully compatible with NGAS’s MMIC production processes

**Frequency bands w/ WLP**

- X-band
- Ku-band
- V-band
- Ka-band
- Q-band
- W-band

**Different circuit types w/ WLP**

- LNAs
- Oscillators
- Shift registers
- PAs
- Phase shifters
- Switches

**Different compound-semiconductor technologies w/ WLP**

- InP HEMTs
- ABCS HEMT
- MEMS switches
- Passives
- GaN HEMTs
- InP HBTs
- GaAs HEMTs
- GaAs HBTs
- GaAs Schottky diodes
- InP diodes

**Substrate combinations w/ WLP**

- GaAs + GaAs
- InP + GaAs
- InP + InP
- Quartz + Quartz
- Si + InP
- Glass + Glass
- GaAs + Duroid
- GaAs + InP + GaAs
- GaAs + InP + InP
- SiC + SiC
- Multiple GaAs integrations
- Multiple InP integrations

NGAS has extensive experience in heterogeneous integration using WLP
Examples of Packaged MMICs

Ku Band PA, WLP GaAs HEMT circuit

Ku Band LNA, WLP GaAs HEMT circuit

Q-Band LNA, WLP GaAs HEMT Circuit

W-Band PA, WLP GaAs HEMT circuit
Wafer Level Packaging (WLP) MMICs Proven across the bands

**KU**
- 4-bit PSHH
  - Chip size: x=3.3mm, y=2.7mm
  - TTL compatible
  - avg RMS Amp Error=1.08dB
  - avg RMS Phase Error=16.5º
- 2-Stage, self-biased LNA
  - Chip size: x=3.3mm, y=2.7mm
  - Bias: 4V, 26 mA
  - Gain > 26.5 dB at 16 GHz

**KA**
- 2-Stage PA
  - Chip size: x=3.3mm, y=2.7mm
  - Bias: 4V, 120 mA
  - Gain > 19 dB at 16 GHz
- 3-Stage, self-biased LNA
  - Chip size: x=4.2mm, y=4.2mm
  - Bias: 4V, 45 mA
  - Gain > 24 dB at 35 GHz

**Q**
- 3-Stage, self-biased LNA
  - Chip size: x=4.2mm, y=4.2mm
  - Bias: 4V, 60 mA
  - Gain > 11.8 dB from 30-50 GHz

Miniaturized WLP T/R modules for large arrays
GaN WLP Technology

- Developed world’s first GaN wafer level package process for record power density
- Demonstrated >99% GaN WLP interconnect yield
W-Band WSA Oscillator

- W-Band oscillator with built-in on chip resonant cavity
- 2-layer active MMIC integration:
  - InP HEMT + GaAs HBT

Measured spectrum of Oscillator

Photo of the integrated oscillator chip
Comparison of WLP and non-WLP circuits

RF performance similar for WLP and non-WLP circuits
2-LAYER INTEGRATED WLP/WSA EXAMPLES
Heterogeneous Integration Example

- Integrated RF front end module with antenna
  - Amplifier (GaAs HEMT)
  - 3 bit phase shifter (GaAs HEMT)
  - Interconnections (ICICs)
  - Antenna
On-Wafer Measured Data

- WLP technology
  - Wafer1 = passive, 4-mil GaAs
  - Wafer2 = 0.1um, 4-mil GaAs
- 2-stage balanced Amplifier
- 3-bit reflective phase shifter

**Amplifier S-Parameter**

**Phase Shifter Phase States**

- Frequency (GHz)
- Magnitude (dB)
- Phase (deg)
- Phase States
WLP Linear Array Demonstration

- Demonstrated fully functional front-end modules with a linear 4-element array
  - GaAs HEMT + passive
  - Amplifier + 3bit PS + antenna in an integrated Q-Band WLP package
  - Successful integration to BFN board
  - Demonstrated electronic beam steering

Integrated RF front-end modules w/ antenna

Measured Beam Pattern

Integrated RF front-end modules w/ antenna

Beam Forming Network (board)

WLP bottom side

WLP top side (antenna)
INTERCONNECTS & TRANSITIONS
RF ICICs

- RF ICIC 50 Ohm Coaxial Transition
- Designed to provide minimal mismatch between 50 Ohm microstrip line (wafer 1) and 50 Ohm CPW line (wafer 2)

Measured Data from RF ICIC Structure
(2 RF ICIC transition + thru line)

Demonstrated Low Loss, RF ICICs
Low Loss RF Vias

- RF via transitions
  - Low loss up to 50GHz
  - <0.1dB insertion loss up to 30GHz

- DC interconnects
  - > 99% yield

- Calibration structures
  - To ensure accurate measurement

Demonstrated Low Loss RF Vias for WLP devices
High Frequency RF Interconnects

- First-of-a-kind W-band WLP RF interconnect
  - Insertion Loss < 0.2 dB
  - Return Loss > 20 dB
  - 20 dB isolation

Demonstrated Low Loss, High Isolation
W-Band WLP Interconnects
Isolation Using Ground Fence

- Isolation fence can be built using 3D interconnects within WSA
- Demonstrated 30dB isolation improvement in W-band using ground fence
- 3D WSA offers design flexibility and performance improvement

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**Simulated Isolation Fence Response**

**Measured Isolation Fence Response**

Blue: no via fence
Red: with via fence

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RF Isolation Design For WSA MMIC
PACKAGE PERFORMANCE
WLP chips **Passed** the many military standard tests:

- **Vibration-Sine**
  - MIL-STD 883F, Method 2007.3, condition B
- **Mechanical Shock (Pyroshock)**
  - MIL-STD 883F, Method 2002.4, condition B
- **Die Shear**
  - MIL-STD 883F, method 2019.7
- **Temperature Cycling**
  - MIL-STD 883F, Method 1010.8, condition B
  - -55°C to 125°C, 50 cycles, MEMS
  - -55°C to 85°C, 300+ cycles, W-Band GaAs circuits
  - -55°C to 125°C, 500 cycles, GaAs PA
- **Hermeticity**
  - MIL-STD 883F, Method 1014.11
  - He fine leak, condition A2, flexible
  - Radioisotope fine leak, condition B
  - Penetrate dye gross leak, condition D

**Environmental test:** 85°C 85% humidity 7 days Ku band GaAs MMICs

WLP packages are hermetic, thermally and mechanically robust
Thermal Robustness

- 24 to 40 GHz GaAs HEMT LNA
- Thermal cycling, -55°C to 125°C
- 500+ cycles

Measured $s_{21}$ response as function of thermal cycles
MULTI-LAYER WLP/WSA
Advanced Integration: Multiple Layer WLP

- Example: 4-layer construction
  - Use bonded pair as starting units

Multiple Layer WSA Flow

Bonded Pair 1

Bonded Pair 2

or single wafer

Process Bonding
layer if necessary (backside)

Wafer Bonding

4-layer Bonding Process Flow

Bonded Pair 1

Bonded Pair 2

ICIC (Front side)

BICIC (backside)

Bonding Layer

4-Layer Construction is Achieved By Bonding 2 bonded WLP pairs
X-Band Tri-Layer Tx/Rx Modules

Average mass: 12.9mg
Size: 2.5mm x 2mm x 0.46mm

• Next-Generation Large Aperture Array T/R Module
  – Ultra light weight (<15 mg)
  – Extremely compact (<5 mm²)

• Transceiver Module Performance
  – FOM > 10,000
  – Reliability: MTTF > 10⁶ Hours
Tri-Layer T/R Demo

- Tri-layer T/R module demonstration
  - GaAs HEMT + InP HBT + InP HEMT
  - Demonstrated excellent yield and T/R circuit performance

Measured NF (Rx) of the tri-layer WLP T/R module
CMOS + III-V Integration Demo

**Input Digital CTRL Waveform**

**Measured Phase Shifter Data**

Demonstrated heterogeneously integrated CMOS flip-chip to WLP MMICs
HIGHER ORDER ASSEMBLY
### WLP Higher Order Integration Demonstrations

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<tr>
<th>Fixture</th>
<th>Alumina</th>
<th>Organic Board</th>
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#### Assembly
- Technologies integrated
  - GaAs-GaAs
  - GaAs-InP
  - InP-InP
  - ABCS-InP-GaAs

- Techniques demonstrated
  - Epoxy to Fixture/Board
  - Bump to Board
    - Manual
    - Auto assembly

#### Demonstrations
- CMOS to III/V Integration
- Direct WLP to Board Attach
- 16-element Ku-band Rx Array
- 8-element Ku-band Rx Sub-Array
- 4-element Q-band Tx Array

#### Benefit
- SWaP reduction
- SWaP, cost reduction
- Near term insertion
- Design to manufacturing
- mmW array implementation

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**Demonstrated WLP-to-Board Integration**
Microbump: Chip-Board Integration

- Developed microbump technologies for WLP-to-board attachment and integration

Microbumps on backside of the package

Sn/Pb microbump array

Cu stud microbump

Microbumps enable direct WLP-to-Board Integration
Direct Board Attach Using Microbumps

X-ray result showing good board to chip interface

Excellent Chip-to-Board Microbump Interface
Example of Epoxy Attach and Ribbon Bonds Implementation

Ku Band subarray board with WLP chips

Integrated Subarray Antenna Board

WLP modules

5 WLP MMIC fixture for environmental testing

WLPs are compatible with epoxy attachment
WLP on Interposer Boards on PWB

Front Side: WLP on Interposer

Back Side (Solder Ball)
WLP on Interposer

WLP Interposer board attachment to PWB
Higher Order Integration Using WLP/WSA

- Demonstrated thermal cycling robustness of WLP-board assembly with underfill
  - >200 cycles
  - from -40C to 100C
  - Pass without failure

- Successfully demonstrated dual side WLP chip-to-board attachment

Chips on the front side of PWB after backside assembly

Chips on the backside of PWB
Summary

- WLP technology offers performance superiority and affordability for next-generation systems
- WLP offers significant size, weight and cost savings for future systems
- Demonstrated multiple advanced technology integration with WLP
- Verified robustness of WLP packaging by MIL-STD tests
- Demonstrated WLP integrated MMICs & modules across the bands
- NGAS is committed to mature and improve wafer-scale integration technology for system insertion